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PHASE I REPORT  
FOR  
A REDUNDANT SPACECRAFT SEQUENCER  
BREADBOARD

FOR THE PERIOD DECEMBER 22, 1965 TO MARCH 30, 1966 .

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## SUMMARY

This report describes work performed under Phase I of JPL subcontract No. 951345. (The Phase I portion of this program has included the completion of design detail for the implementation and test of a redundant spacecraft sequencer breadboard.) The sequencer is a redundant version of a portion of the Mariner C Spacecraft Sequencer as described previously in the Task II report of JPL subcontract 950777, "Design Study for a Redundant Spacecraft Sequencer." The preparation of design detail included the circuit design and circuit testing required to insure the intended performance of special circuits, and the establishment of test plans to verify the performance of the breadboard systems. The Phase II portion of this program will include the actual construction and test of the breadboard system.

This work was performed for the Jet Propulsion Laboratory, California Institute of Technology, sponsored by the National Aeronautics and Space Administration under Contract NAS7-100.

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## 1. INTRODUCTION

This report is the Phase I report in a two phase program for the fabrication and test of a Redundant Spacecraft Sequencer. This program is a follow-on to a previous design study performed by Westinghouse on JPL subcontract 950777. (In the design study, a computer synthesis procedure was used to design a redundant version of the Central Computer and Sequencer of the Mariner C spacecraft. This equipment was to be subject to all of the functional requirements of the non-redundant central computer and sequencer plus the following additional requirements:

1. No single component failure could cause the failure of any critical event output.
2. The equipment was required to be non-volatile so that in the event of a power failure it would not lose significant information and would resume operation in the usual manner when power was restored.)

The basic function of the central computer and sequencer is to provide timing signals to other subsystems of the spacecraft. These signals are primarily in the form of relay closures and are used to control the spacecraft midcourse maneuvers, as well as to initiate other events which occur throughout the mission. The study resulted in an equipment design which promises to afford a significant reliability improvement over an equivalent non-redundant equipment. This improvement is achieved with very little weight increase over that required by basic triplication of the non-redundant circuitry. [The design makes use of multiple-line logic, with three copies

of each logical design and majority voting circuits at selected points to remove the effects of errors.]

The breadboard model, which will result from the present contract, will be used to verify the results of the design study and demonstrate the effectiveness of the redundancy. The breadboard includes the electrical equivalent of a significant portion of the entire redundant sequencer. Low density packaging is used to reduce costs and to permit a comprehensive testing program to be performed. The circuitry is a combination of integrated and discrete component circuits. The first phase of this program involved the finalization of the breadboard design and establishment of an effective test plan. The second phase includes the fabrication and testing of the system.

A simplified block diagram of the portion of the central computer and sequencer which is of interest to the present effort is shown in Figure 7-1. The output of a 38.4-kc crystal oscillator timing source is fed into a divider chain. The divider chain provides signals with frequencies 20 pulses per second, one pulse per second, and one pulse per minute. Finally, the one pulse per minute signal is fed into the Launch Counter. The latter provides the signals associated with events occurring immediately after launch. The figure also indicates the test chassis and digital difference detector circuitry used to test the redundant equipment.

The model is being constructed in accordance with the details of the previous design study. In accordance with the design, the primary redundancy technique to be employed will be multiple-line majority voted logic.

This technique requires the use of three replicas of each function appearing in the non-redundant version of the equipment. At selected locations, sets of majority voters (restorers) are inserted at the outputs of the replicated functions. The sets of voters compare equivalent signals and remove the effects of any minority of errors. The outputs of the majority voters are used as the replacements of the output signals of the associated functions.

In addition to the use of multiple-line logic, special circuits are utilized to satisfy requirements peculiar to the redundant system configuration. Among these are those required for providing a redundant clock source, testing the redundant equipment, maintaining synchronization between the multiple replicas, providing reliable power supplies, and maintaining high reliability at the interface between redundant and non-redundant subsystems.

The primary efforts during Phase I of this contract were directed toward the following areas:

- (1.) Establishment of the mechanical configuration for the breadboard system.
- (2.) Updating of the system design.
- (3.) Circuit design and circuit design verification.
- (4.) Test equipment design.
- (5.) Establishment of test plans.
- (6.) Preparation of documentation.

Details of the accomplishments in each of these areas are given in the following sections.

## 2. MECHANICAL CONFIGURATION

The mechanical configuration for the breadboard system is shown in Figure 7-2, "Redundant Sequencer and Test Chassis." The sequencer chassis, shown on the left is a conventional 3 row card rack with a total of 99 printed circuit card locations, for 3 X 4 inch cards. All multiple-line logic will be implemented using printed circuit cards located within the card rack. All logic associated with one replica of the triplicated logic will be located within a single card row. In addition to the multiple-line logic, the card rack will also contain digital difference detector cards which are used only for test purposes. All component redundant circuitry, such as the clock source, regulators and power distribution, will be located on a panel attached to the back of the card rack. The component redundant circuitry will utilize breadboard construction techniques, rather than printed circuitry, to allow ready access to components and wiring.

The above configuration for the sequencer chassis provides maximum accessability to the component redundant circuitry and also provides a high degree of accessability to the multiple-line logic. Test points, located at the top of each printed circuit card, allow monitoring of individual circuit outputs on the cards. Extender cards will be supplied which will allow individual printed circuit cards to be operated with their components completely accessable. The extender card will have provisions for "opening" individual printed circuit input and output leads. The sequencer chassis

will be provided with a dust cover as shown in the illustration.

The test chassis, shown in Figure 7-2, will contain all input-output controls and indicators required for the operation and test of the sequencer. In addition, the test chassis will contain the DC power supplies required by the system. The test panel will include a system block diagram overlay so that all controls and indicators can be directly associated with their respective sections of the system. The test chassis will be electrically connected to the sequencer chassis via a cable approximately 10 ft. long.

### 3. SYSTEM DESIGN UPDATING

A brief description of system changes and additions, that have been made since the design study Task II report, is given in the following paragraphs:

As required by the purchase description for this contract, the frequency of the redundant clock source has been changed from 9.6 KHZ to 38.4 KHZ and a divide-by-four counter has been inserted between the clock source and the divide-by-480 counter. (Shown in Figure 7-6 in its non-redundant form). It consists simply of a 2 bit ring shift register with inversion between the last bit and the first bit. The resulting shift register counter sequences thru all four possible states before recycling. Each bit changes from the "0" state to the "1" state and back only once during a cycle so that the output is a 9.6 KHZ square wave. A majority voter is placed in the feedback loop, of each counter, which provides synchronization between replicas and the required majority voted output. The counters will always be synchronized after two clock pulses.

The divide-by-480 counter has been redesigned to use integrated circuit flip-flops rather than magnetic memory elements. This change was made as a result of the following considerations:

- (1.) non volatility is not required for this counter
- (2.) the power dissipation in the magnetic elements is relatively high at the operating frequency of this counter
- (3.) integrated circuits are smaller and do not require special

driver and buffer circuits. The integrated circuit version of the divide-by-480 counter is shown in Figure 7-7. The logical configuration is basically the same as the previous magnetic version except that the set driver has been eliminated. The synchronizing signals used to set the counters to their initial status are now derived from the following divide-by-20 counters rather than from the divide-by-480 voters via set drivers. The signals from the divide-by-20 counters have the required delay for proper setting of the initial states. Note that a more optimum configuration for the divide-by-4 and divide-480 combination could probably be made, especially if the 9.6 kc signal were not required as a system output.

Several alternatives for the elimination of the +12V.DC regulated power supply were suggested in the Task I report of the design study. The redesign of circuitry associated with the magnetic registers has eliminated the need for +12V. regulated power in the breadboard system. The primary change was redesign of the shift driver so that it could produce a +12V. transfer pulse while operating from a +6V. power source. The new design of the shift driver is discussed in the next section of this report.

As specified in the purchase description, the breadboard system will operate from 60 cps. primary power rather than 2.4 kc square wave primary power as described in the design study. The design of 60 cps. to 2.4 kc. converter for operation of the breadboard could not be justified, therefore a power system was designed which utilizes conventional 60 cps. power supplies. The new power system is similar to the previous system except that the effective primary power to the redundant power distribution circuitry for the sequencer is now D.C. power. This decision resulted in a minimum of change to the existing redundant regulator design. The details of the redundant power distribution circuitry are described in the next section of this report.

In the original design, power was applied continuously to the voters. However, power was applied only during the shift pulse to the logic gates. The switched gate power provides a considerable savings in the average power dissipation. A suitable method of providing switched power to the voters was not developed during the design study. However, a method has now been developed and has been included for all voters associated with the low speed (i.e. magnetic) counters. The delayed power switches for the voters are enabled by the OR of the shift pulses from all three replicas so that the voter output will be correct even if the associated shift pulse has failed. Additional information on the voter delayed power switch is included in Section 4.2 of this report.

The update enable signal to the launch counter, as shown in the Task II report of the design study, was used to prevent all registers except the

7 state ring from shifting during update. The update enable is also applied to various control gates in the launch counter to inhibit inputs to registers other than the 7 state ring and to enable the 7 state ring overflow. Two changes have been made to this circuitry. Since it is now assumed that the launch counter will not be updated in flight, the launch counter will be in its cleared state during update. Therefore it is not necessary to divert shift current during update in order to maintain counter states. Secondly, the original connections of the update enable to the control gates were not entirely correct and these connections have been corrected.

Although the purchase description states that the launch clamp function will not be included, a simulated launch clamp signal or its equivalent is required to prevent the L-2 and L-3 relays from setting on the first clock pulse after the release of count inhibit. Therefore, in the breadboard model the clear and counting signal will be used as a simulated launch clamp.

#### 4. CIRCUIT DESIGN AND VERIFICATION

##### 4.1 REDUNDANT CLOCK SOURCE

Several circuit configurations, for the redundant clock source have been tested in the laboratory. The circuit which provided the best performance, and will be used in the sequencer, is shown in Figure 7-15. The oscillator circuit shown in the figure is basically the NAWEPS 16-1-519-2 Preferred Circuit PSC 31 with some modifications to meet the requirements of the redundant system. The circuit is recommended for crystal oscillators

in the 20 to 100 KHZ regions. The circuit is an amplified feedback type of oscillator in which the feedback path is from the collector of Q2 to the base of Q1 through the crystal. The impedance of the crystal at series resonance is low enough to permit feedback of sufficient amplitude to start and maintain oscillations over the temperature range. The output signal from the oscillator at the collector of Q2 is a square wave with a good drive capability. Therefore, an additional stage of buffering, as used in the previous circuit was not required. The oscillator outputs are summed, as before, for each of the three replicas in the system and the load is driven via a buffer and squaring circuit. The oscillators are synchronized to each other via capacitors which connect the bases of the Q1 transistors.

The original redundant oscillator design, as described in the Task I report of the design study, did not operate satisfactorily with the 38.4 KHZ crystal. The crystal which is being used is the Reeves-Hoffman, type 13N3, 38.4 KHZ  $\pm 0.01\%$ , crystal as specified in the purchase description. The circuit was quite critical with respect to capacitor values and the build-up time, after turn-on, was very long. It appeared that the crystal impedance was too high at the frequency required for oscillation.

A modified version of the original circuit was then built which included an inductor. The diagram of this circuit was in the set of reproducible drawings previously submitted to JPL. The inductor was added to provide additional phase shift so that the frequency of oscillation would become closer to the minimum impedance point of the crystal. This circuit, however, was still critical and required an extra buffer at the output of the oscillator.

It was then decided that a two transistor oscillator would provide more reliable operation and the circuit of Figure 7-15 was constructed. As indicated previously, the two transistor circuit has provided the best performance of those tested. The redundant circuit operates quite satisfactorily with any single component either opened or shorted. However, there are indications that if one of the crystals were to fail such that one of the oscillators begins oscillating in a relaxation mode, the failed oscillator might pull the other oscillators out of synchronization. This problem should receive further investigation, however, it is beyond the scope of the present contract.

#### 4.2 NS2 CARD-SHIFT DRIVER, DELAYED POWER SWITCH AND RC CIRCUIT

Printed circuit card NS2, shown in Figure 7-16, contains the shift driver, shift voltage source and power switches. The shift driver is a monostable circuit which provides the two outputs required for the operation of the gated core-diode magnetic shift registers. The shift output provides the high current pulse for the magnetic core readout. The transfer output is a voltage pulse that allows the magnetic register capacitors to remain charged for the duration of the shift pulse; it returns to ground after the shift current pulse has ceased; this enables the magnetic register outputs (as well as the logic output for the first bit) to be stored into the appropriate bits of the magnetic register. The power switches provide power to logic gates, voters, and the register input circuits only during the transfer pulse. The shift voltage source is a simple R-C network to provide the source of the shift current. It is designed to minimize power

supply loading, to gradually reduce the amplitude of the shift current pulse, and to provide a low current source for the reset and clear inputs.

The shift driver is activated by grounding an input to charge a small input capacitor through a high impedance path. The shift driver is triggered when the input ground is removed and the capacitor discharges through a low impedance path which includes a zener diode to set the trigger threshold. Once the input circuit has triggered, the in-phase output signal is fed back through a timing network to maintain the shift driver in the ON state for the desired period of time. The shift output is a current limited transistor stage which saturates if less than the maximum current at a positive voltage is available from the shift source. The transfer output is driven by a complementary (PNP-NPN) inverter stage in which neither transistor is conducting during the quiescent period. During the period that the shift driver is ON, the transfer output is driven by a low impedance to a voltage slightly less than twice the supply voltage (approx. 10V.). This double voltage is supplied by a capacitor which cannot discharge to a level below the supply voltage. The transfer output is driven to a low impedance to ground when the shift driver switches OFF, but the low impedance to ground is maintained only for a short period of time. A shunt resistor to ground provides a relatively high impedance path to ground for leakage currents during the quiescent period.

The delayed power switches are driven from one (or all three) of the transfer outputs from corresponding shift drivers. The delayed power switch output is simply a low impedance to the voltage supply during the transfer pulse, with a slow rise time to control decoder "spiking". Delayed power

switching is used on all logic gates and voters in the magnetic logic to reduce the power requirements. The switched power output is also used for the magnetic register input circuit to provide a relatively constant charging voltage for the input capacitor.

As described above, the shift voltage source is a simple R-C network. Energy for the shift current is stored in the capacitor; the resistor limits the current drawn from power supply to that used for clear and reset. Because the shift driver is ON for a longer time than required for read out of the magnetic bits, the capacitor value is chosen so that it becomes discharged during the shift pulse.

The circuit configurations for the shift voltage source and delayed power switches are essentially the same as previously proposed. The use of power switching for the majority voting, however, is new. Each voter power switch has a diode OR gate input from all replicas of the same transfer pulse so that no failures propagate through voters. The voter power switch has a longer time constant to provide longer turn-on delay and insure elimination of spiking. The voter power switch does not have a fast turn-off because it is not necessary and cannot be implemented in the simple manner used for the logic power switch without causing failure propagation through voters.

The shift driver, however, has been significantly redesigned from its previous configuration. The primary areas of design change are:

1. Redesign to an all-semiconductor configuration with resistor and capacitor passive components.
2. Design of a voltage doubler to provide a higher transfer voltage

from a single low-voltage power source.

3. Redesign of input triggering circuit to provide protection against false triggering on power transients, input noise immunity and integration of inputs to improve rejection of possible spurious inputs.

The first design task was the elimination of the magnetic transformer and the use of the transfer output for driving the shift current driver and the timing circuit.

The voltage doubler circuit was designed to use a capacitor (normally charged to power supply potential) in series with the power supply during the shift pulse to provide the positive supply for the PNP transistor switch during the transfer pulse. Some "droop" on the transfer pulse is quite permissible because the highest voltage is necessary only during the magnetic readout in the early portion of the shift pulse. The voltage level of the transfer pulse is approximately 1 to 2 volts less than twice the power supply voltage. The input triggering circuit was redesigned to eliminate or reduce the possibility of false triggering. The use of an input capacitor normally discharged in the quiescent state (regardless of power level) and a Zener diode threshold eliminates the possibility of triggering on power transients (including power turn-on) and provides improved noise immunity when compared to the previous configuration. The coupling capacitor was reduced in value and a comparatively long time constant charging path is used which requires an input pulse of significant duration before enough voltage is stored in the capacitor to exceed the threshold of the Zener diode. The exact levels and duration required to trigger the driver depend,

of course, upon the power supply voltage, with triggering becoming progressively more difficult as power supply voltages are lowered to the minimum operating voltage. Other minor changes to the transfer output of the shift driver include the deletion of the current limiting resistor (there is no regeneration in this circuit if there is a fault on the transfer line which prevents it from rising above ground), as well as minor modifications to the trigger circuit for the NPN transistor to limit charging current and improve noise immunity.

#### 4.3 NS3 CARD, MAGNETIC REGISTERS

Printed circuit card NS3, shown in Figure 7-17, contains five individual gated core-diode magnetic shift registers. These registers are the non-volatile storage elements of the sequencer system. Each core of the magnetic register provides one bit of shift register storage. An input circuit is included for each register so that a logic signal may be used to set the first bit of the register. The input circuit, therefore, provides the semiconductor logic -- magnetic register interface.

The operation of gated core-diode shift registers is basically summarized as follows: Each core is wound with at least 3 different windings -- a high current shift winding and two low current windings, one each for read-in and read-out. In addition, the first core is sometimes provided with an alternate shift winding which is wound in the opposite sense to permit setting the first core while clearing all remaining cores. Every core also has diodes in series with the read-out and read-in windings, and an output capacitor. Information is shifted through the register by

the two-step operation of read-out, then read-in. Shift current provides the read-out operation by providing a sufficiently high reset current to provide a corresponding induced current in the read-out winding of any core not previously reset. This current flows through the read-out diode and charges the output capacitor. No current flows in the input winding if the transfer voltage is sufficiently high to reverse bias the read-in diode. There is, however, an induced voltage in the read-in winding approximately equal to the voltage on the output capacitor of the same core. The output capacitor remains charged until the transfer line is grounded; this causes any of the charged capacitors to discharge through the read-in winding and set the corresponding core. Any current flow through the read-out winding at this time is prevented by the read-out diode.

The magnetic register input circuit simply provides an additional output capacitor which is discharged through the input winding of the first bit. In addition, there is a capacitor charging resistor and a pullup resistor connected to the switched power voltage clamp from the shift driver. The capacitor is charged if a logical "0" ground is present on the input during the transfer pulse. A diode is included to insure a low impedance discharge path.

There have been no significant changes in the circuit configuration of the magnetic register or the input circuit. The entire magnetic register is a vendor-supplied pre-packaged unit.

#### 4.4 NS4 CARD-BUFFERS

Printed circuit card NS4, shown in Figure 7-18, contains the buffers for the magnetic register semiconductor interface. The buffers provide a high impedance load to the magnetic register outputs. Input to the buffers is through a diode OR gate. A logical "1" can be guaranteed on the buffer output by grounding the OR gate output through one or more diodes provided for that purpose.

The basic buffer circuit consists of 3 stages - a positive logic OR gate driving an emitter follower which drives an inverter output stage. Any positive input will cause the output to be a logical "0". However, if one of the inhibit inputs is grounded, this causes all inputs to be a logical "0" and therefore forces the output to be a logical "1". In addition, a high impedance discharge path is provided from the OR gate output and is to be connected to the transfer output of the shift driver.

The discharge path is the only significant change in the buffer circuit. This path allows removal of charge from any magnetic register output capacitor not discharged by the transfer voltage (the last bit of every complete register has no other discharge path), and also provides a path for any leakage current.

#### 4.5 NS5 CARD-POWER FAILURE DETECTOR AND SET DRIVER

Printed circuit card NS5, shown in Figure 7-19, contains the power failure detector and a set driver. The power failure detector inhibits the possible passage of count pulses down the divider chain when power supply conditions are such that improper logic operation might result. The power

failure detector operates as a functional part of the divide-by-20 counter by immediately inhibiting the one pulse per second output after either the loss of AC power or the restoration of DC power to the logic. The set driver circuit is used to insert the initial state in the divide-by-60 key stream generator register. It is activated by the restored output decoder and forces the register to contain the initial state (regardless of the previous state) after the end of the shift current pulse. The circuit configuration of the basic set driver has not been changed significantly. A PNP emitter follower has been added to the input to reduce the input current load. A small resistance has been added to the input charging path to limit current and require an input pulse of significant duration for triggering. Another resistor has been added from the input side of the timing capacitor to ground to improve noise immunity. Although there is no regeneration, the normal power supply input has been buffered to further insure that power supply transients cannot cause spurious outputs.

The power failure detector has been significantly redesigned to make it compatible with 60 Hz sinusoidal input power. Timing and storage capacitors were increased to compensate for the greater filtering capacity of the DC supplies used for the breadboard and the longer period of uncertainty of primary power failure, compared to the 2.4 KHz square wave source for the actual spacecraft sequencer. In addition, laboratory testing showed that the amount of 120 Hz ripple on the primary AC power supply for the failure detector results in multiple switching of the inhibit output after power turn-on. This is caused by the requirement for a long time constant from the DC supply and a minimum of filtering on the primary

AC power supply. This problem was solved by using two independent circuits to provide the inhibit output: one is specifically designed for loss of primary power; the other provides the turn-on inhibit. Also, the diode input for the count inhibit is located on the power failure inhibit card as a matter of convenience.

#### 4.6 NS6 CARD-RELAY DRIVER AND DIODE ARRAY

Printed circuit card NS6, shown in Figure 7-20, contains a relay driver, relay, and a diode array. A negative-going signal on any driver diode input causes the circuit to turn ON and remain ON for a fixed period of time. The set coil of the magnetically latching relay is energized during this time. A direct input which causes the circuit to be ON continuously, and manual controls for setting and resetting the relay are also provided.

The relay driver circuit is essentially a monostable PNP-NPN two stage inverter with capacitor coupling to the first stage from either the output or the diode inputs. A special direct-coupled input is provided which is used for the Launch Clamp. Grounding this input causes the circuit to remain ON and completely discharge the output capacitor, thereby preventing any further setting of the relay until the clamp has been released and the output capacitor allowed to charge. Grounding any input diode causes the circuit to turn ON and the output capacitor to discharge through the set coil of the relay. The feedback is coupled to the input through another diode, so that the input may be released at any time during the output pulse without affecting the output. Even if a diode input remains grounded,

the circuit returns to the OFF condition. This permits manual setting of the relay, even though another diode input will not trigger the circuit.

The primary changes in the circuit of the relay driver involve the use of 6V. power and the configuration of the input circuit. The use of 6V. power eliminates the requirement for the Zener diode formerly used, and therefore eliminates the problems associated with the tolerance on the 28V. and 6V. power supplies and on the Zener diode threshold. The circuitry was also simplified to use a single timing network for both the input feedback and the input triggering. The coupling capacitor is normally discharged, with both sides referenced to the 6V. supply (which is connected to the emitter of the first stage), so that power supply transients (including power turn-on) do not trigger the circuit. The addition of a small integrating capacitor (also referenced to the 6V. supply) improves the input noise immunity and the rejection of possible spurious inputs.

#### 4.7 STANDARD CARDS

The standard printed circuit cards, as shown in Figures 7-22, 7-23, 7-24 and 7-25, contain line drivers, gates and flip-flops which are compatible with the sequencer system. The positive logic driver of Figure 7-22 is essentially a 3 input NAND gate capable of driving 100 ma. bilateral current for 6V. and +6V. logic levels. Signal returns are provided for each signal output. The circuit is capable of withstanding temporary short circuits to ground at the output when all inputs are logical "1". The positive logic driver is used in the sequencer as the line driver to ground support equipment.

The NAND gate and flip-flop cards shown in Figures 7-23, 7-24 and 7-25 contain convenient arrangements of diode-transistor integrated circuits. The integrated circuits are MLL tested versions of the Westinghouse and Raytheon 200 series line, in TO-5 can packages.

#### 4.8 REDUNDANT POWER DISTRIBUTION

The sequencer power distribution system is shown in Figure 7-14. The primary power, as received by the sequencer breadboard, is DC power from the test chassis distributed on redundant lines. The +28V. power, for the relays, is received on 3 lines into a diode buffered node. The voltage at the node will be the highest of the three applied voltages. Note that the node connection can be disconnected so that different voltages can be applied, via the test chassis, to each replica. The power is fed from the node (via decoupling networks consisting of a fuse, diode, capacitor and bleeder resistor) independently to each replica of the system. The +6V. power distribution is similar to the +28V. power distribution except that, the +6V. power is regulated power. The redundant power regulator shown accepts +12V. power from the test chassis and provides +6V. power to the sequencer system. The regulator is designed so that no single component failure can cause the output voltage to fail high. The regulator design is basically the same as previously proposed. The regulator circuit, shown in Figure 7-14/2 provides very good regulation over the required temperature, loading, and input variations, as well as with single failures.

The regulator was tested over the temperature range from -10°C to +95°C, with an input voltage variation from +10V. to +15V., with an output

load variation from 0 ma. to 333 ma. and with simulated single component failures. The output current and voltage of the regulator was measured on the load side of the fuse and decoupling network. A minimum output of 5.04 V. was obtained with the minimum input voltage, a temperature of  $-10^{\circ}\text{C}$  and maximum load. A maximum output of 7.18 volts was obtained with the maximum input voltage, a temperature of  $+95^{\circ}\text{C}$  and minimum load. A bleeder resistor in the decoupling network maintains a minimum drain of 90 ma. thru the output diodes to prevent loss of regulation in the diodes.

The +6 V. power requirements for each replica are broken into two parts each part of which is fed via a separate decoupling network from the +6 V. node. The power sense signal, which indicates the imminent failure of +28 V. and +6 V. power is derived from a special DC supply in the test chassis and is fed from the power sense node to the power failure detectors in the divide-by-20 counter circuitry.

## 5. TEST EQUIPMENT DESIGN

The test equipment developed during Phase I includes: 1.) the digital difference detector cards, 2.) the extender card and 3.) the test chassis. In addition however, minor changes were made to the original logic design in order to accommodate the forcing signals required for test. Control inputs were added to each replica to permit all processors ~~outputs~~ ~~in~~ a replica to be forced to a continuous "1" or continuous "0" state. These forcing controls are required to implement the single rank testing capability used to locate failures that would be masked by the triple redundancy. Control inputs were also added to permit all voter outputs in a replica to be forced to a continuous "1" or continuous "0" state. The voter forcing was added to facilitate voter testing. The procedure used to obtain the "0" and "1" outputs is as follows:

1.) The "0" outputs are obtained by simply grounding the output line via an additional diode or gate.

2.) The "1" outputs are obtained by grounding an input to the output gate. In some cases an existing input is grounded via a diode and in other cases, separate gate inputs are utilized.

Descriptions of the ~~digital difference detector, extender card and~~ test chassis are provided in the next sections.

### 5.1 NS7 CARD-DIGITAL DIFFERENCE DETECTOR

Printed circuit card NS7, shown in Figure 7-21, contains the digital difference detectors used for the testing of the sequencer breadboard.

These circuits were added as part of the test equipment and do not contribute to the functional operation of the sequencer. The difference detector card also contains connections for the forcing signals so that these controls are mechanically disconnected from any of the associated signals if the difference detector card is removed. The entire set of difference detectors permits complete checking of the logic redundancy of the sequencer. The difference detectors themselves are not triplicated; only one detector is associated with each voter input and voter output.

Two sets of diode gate inputs detect both the highest and lowest voltage input. If the highest exceeds the lowest by the threshold of the circuit, the detector transistor is turned on. If the lowest input under these conditions is also near ground (logical "0"), then the difference detector output becomes a logical "1". If the display control input is a "1", then any difference that persists for a minimum amount of time will activate a logical feedback connection which will maintain the output at a logical "1". The minimum time required to latch the output is primarily determined by the integrating capacitor on the node of the feedback gate.

## 5.2 NS8 CARD-EXTENDER

The NS8 Extender Card is a special extender card which includes a patch panel between the input and output connectors. The card will allow the operator to open or short any circuit point which passes thru a card connector without unsoldering leads or disturbing the connector wiring. The extender cards also permit individual printed circuit cards to be operated with their components completely accessible.

### 5.3 TEST CHASSIS

The test chassis front panel is shown in Figure 7-2 and the test chassis schematic is shown in Figure 7-13.

The test panel contains a block diagram of the sequencer, on which the test input switches and output lights are located. In addition to the inputs and outputs normally required by the sequencer for operation, the test panel contains the difference detector indicators and forcing switches required to check for and locate internal failures which would be masked by the triple redundancy. Difference detector indicators located at each voter and processing element. Voter and processor forcing switches are provided for each replica.

The difference detector indicators indicate any significant differences between outputs of corresponding processors and voters in the triplicated system. The difference detector indicators operate in two modes, latching and non-latching, as determined by the difference detector latch switches.

The forcing switches allow the operator to force all processor and/or voter outputs in a given replica to "one" or "zero". This capability allows the operator to test replicas, voters and difference detectors. Thus, to test replica C the processor outputs of replica A are forced to be different than the processor outputs of replica B. Replica C then determines the voter outputs. The combination of difference detectors and single rank testing provides the operator with a convenient method of detecting and locating all failures in the triplicated system.

In addition to the controls and indicators, the test chassis contains the D.C. power supplies for the breadboard system, as indicated in the schematic.

A complete listing and description of test chassis controls and indicators is given below:

1.) Test Panel Switches -

- S-1 Processor Difference Detector Latch (determines whether Processor Difference Detector Lights will be latched on after one difference detection or will be free to go ON and OFF, providing an instantaneous indication).
- S-2 Processor Forcing Switch, Rank A (forces a constant logical 1 or output on all replica A Counters; is open in normal operation)
- S-3 Processor Forcing Switch, Rank B (similar to S-2)
- S-4 Processor Forcing Switch, Rank C (similar to S-2)
- S-5 Voter Difference Detector Latch (similar to S-1)
- S-6 Voter Forcing Switch, Rank A (forces a constant logical 1 or 0 output on all replica A Majority Voters; is open in normal operation)
- S-7 Voter Forcing Switch, Rank B (similar to S-6)
- S-8 Voter Forcing Switch, Rank C (similar to S-6)
- S-9 Count Inhibit, Rank A (inhibits the replica A - 20 Counter stopping all following replica A Counters if the Inhibit Release switch is in the inhibit position)
- S-10 Count Inhibit, Rank B (similar to S-9)
- S-11 Count Inhibit, Rank C (similar to S-9)
- S-12 X20 Speed-Up (effectively by-passes - 20 Counter in all replicas)

- S-13 Clear, Rank A (clears first  $\div 60$  and all following replica A  
Counters)
- S-14 Clear, Rank B (similar to S-13)
- S-15 Clear, Rank C (similar to S-13)
- S-16 X60 Speed-Up (effectively by-passes first  $\div 60$   
Counter in all replicas)
- S-17 Update, Rank A (provides one-shot pulse to replica A  
Launch Counter, simulating normal Launch Counter input signal)
- S-18 Update, Rank B (similar to S-17)
- S-19 Update, Rank C (similar to S-17)
- S-20 Update Enable, Rank A (inhibits  $\div 17$  and second  $\div 60$   
Counter in replica A; for use when Up-dating  $\div 7$  Counter)
- S-21 Update Enable, Rank B (similar to S-20)
- S-22 Update Enable, Rank C (similar to S-20)
- S-23 Set L-1 Relay, Rank A (sets replica A L-1 Relay)
- S-24 Set L-1 Relay, Rank B (similar to S-23)
- S-25 Set L-1 Relay, Rank C (similar to S-23)
- S-26 Reset Relays, Rank A (resets all replica A Relays)
- S-27 Set L-2 Relay, Rank A (sets replica A L-2 Relay)
- S-28 Set L-2 Relay, Rank B (similar to S-27)
- S-29 Set L-2 Relay, Rank C (similar to S-27)
- S-30 Reset Relays, Rank B (similar to S-26)
- S-31 Set L-3 Relay, Rank A (sets L-3 Relay in replica A)
- S-32 Set L-3 Relay, Rank B (similar to S-31)

- S-33 Set L-3 Relay, Rank C (similar to S-31)
- S-34 Reset Relays, Rank C (similar to S-26)
- S-35 A.C. Power (a-c power switch for all d-c supplies)
- S-36 28v D.C., Rank A (connects 28v input of replica A  
to 28v supply or to Test Chassis test point)
- S-37 28v D.C., Rank B (similar to S-36)
- S-38 28v D.C., Rank C (similar to S-36)
- S-39 12v D.C., Rank A (connects 12v input of replica A to  
12v supply or to Test Chassis test point)
- S-40 12v D.C., Rank B (similar to S-39)
- S-41 12v D.C., Rank C (similar to S-39)
- S-42 8v D.C. (connects Power Sense input node of all  
Power Failure Detectors to unregulated d-c supply or to  
Test Chassis test point)
- S-43 8v D.C. (identical to S-42)
- S-44 Inhibit Release (controls the Count Inhibit switches S-9, S-10  
and S-11; if the three Count Inhibit switches are in the  
inhibit position, the Inhibit Release switch serves as a  
master inhibit control for all the replicas by releasing the  
Inhibits simultaneously)

## 2.) Test Panel Lights

- DS-1     $\div$  4 Counter (turned on by Difference Detector Circuits,  
         indicating difference in output between any  $\div$  4 Counters;  
         can give instantaneous indication or be latched on by first  
         difference detection)
- DS-2     $\div$  4 Voters (turned on by Difference Detector Circuits, indicating  
         lack of agreement of any  $\div$  4 Majority Voters; can give instan-  
         taneous indication or be latched on by first difference detection)
- DS-3     $\div$  480 Counters (similar to DS-1)
- DS-4     $\div$  480 Voters (similar to DS-2)
- DS-5     $\div$  20 Counters (similar to DS-1)
- DS-6     $\div$  20 Voters (similar to DS-2)
- DS-7     $\div$  60 Counters (similar to DS-1, for first  $\div$  60 Counters)
- DS-8     $\div$  60 Voters (similar to DS-2, for first  $\div$  60 Voters)
- DS-9    1PPM, Rank A Voters (Toggles at rate determined by output of  
         first  $\div$  60 Majority Voter in replica A, providing visual  
         indication of replica operation; turned off by Clear S-12)
- DS-10   1PPM, Rank B Voters (similar to DS-9; turned off by Clear S-13)
- DS-11   1PPM, Rank C Voters (similar to DS-9; turned off by Clear S-14)
- DS-12    $\div$  7 Counters (similar to DS-1)
- DS-13    $\div$  7 Voters (similar to DS-2)
- DS-14    $\div$  60 Counters (similar to DS-1, for second  $\div$  60 Counters)
- DS-15    $\div$  60 Voters (similar to DS-2, for second  $\div$  60 Voters)
- DS-16    $\div$  17 Counters (similar to DS-1)

- DS-17    ÷ 17 Voters (similar to DS-2)
- DS-18    Up-Date Verify, Rank A (toggles at rate determined by the  
         replica A Launch Counter Input signal when Up-Date Enable  
         S-19 is in Enable Position)
- DS-19    Up-Date Verify, Rank B (similar to DS-18 with S-20)
- DS-20    Up-Date Verify, Rank C (similar to DS-18 with S-21)
- DS-21    1P/7 Hr., Rank A (toggles at rate determined by replica A  
         Launch Counter)
- DS-22    Clear and Counting, Rank A (turned OFF by replica A  
         Launch Counter exactly two minutes after counting has begun  
         provided all Counters were cleared prior to starting the  
         sequence and all Counters function properly; turned ON  
         by Clear S-12)
- DS-23    1P/7 Hr., Rank B (similar to DS-21)
- DS-24    Clear and Counting, Rank B (similar to DS-22; turned off by S-13)
- DS-25    1P/7 Hr., Rank C (similar to DS-21)
- DS-26    Clear and Counting, Rank C (similar to DS-22; turned off by S-14)
- DS-27    L-1 Relay, Rank A (turned on by setting of replica A L-1 Relay)
- DS-28    L-2 Relay, Rank A (turned on by setting of replica A L-2 Relay)
- DS-29    L-3 Relay, Rank A (turned on by setting of replica A L-3 Relay)
- DS-30    L-1 Relay, Rank B (similar to DS-27)
- DS-31    L-2 Relay, Rank B (similar to DS-28)
- DS-32    L-3 Relay, Rank B (similar to DS-29)
- DS-33    L-1 Relay, Rank C (similar to DS-27)

DS-34 L-2 Relay, Rank C (similar to DS-28)

DS-35 L-3 Relay, Rank C (similar to DS-29)

DS-36 Power (turned on with a-c power)

## 6. TEST PLAN

The test plan, as previously submitted, includes a normal operation test (start-up procedure), single rank testing, power drop-out testing and temperature and voltage variation testing. The start up and the single rank testing procedures are discussed in the following sections:

### 6.1 Start-Up Procedure

The start-up procedure which follows is an operational test of the Sequencer Model under conditions corresponding to those of the actual spacecraft sequencer.

If it is desired to prevent the setting of any of the output relays, the +28V power may be switched off to simulate the LAUNCH CLAMP in the actual spacecraft sequencer. Since there is no Agena (or other final stage) separation to generate LAUNCH CLAMP in the normal launch sequence, the Sequencer Model has been designed to include a relay inhibit derived from the CLEAR AND COUNTING signal. However, all relays will set if the +28V has been on prior to the clearing of the CLEAR AND COUNTING flip-flop. The +28V power must be on at least 5 seconds before any output is expected to set a relay.

In order to stop the counting action of the lower frequency sections, the COUNT INHIBIT is applied. This should stop all outputs except the

clock source, 9.6 KHz, and 20 Hz outputs. As indicated, each of the three replicas may be inhibited independently unless the INHIBIT RELEASE switch is on. This switch will release all of the COUNT INHIBITS and allow simultaneous initial operation of the counters.

Since the normal starting condition of all of the lower frequency counters is the clear state with all relays reset, the CLEAR is switched on prior to the COUNT INHIBIT release. The CLEAR should extinguish the 1 MINUTE, 7 HOUR, and UPDATE VERIFY indicators and cause the CLEAR AND COUNTING indicator to light. The output relays are reset by the MANUAL RESET switches. In addition, the DIFFERENCE DETECTOR indicators may be switched to LATCH OFF at any time to extinguish any indicator still set due to previously existing differences.

The X20 and X60 SPEEDUP control switches should be OFF to provide outputs at the normal frequency. Either or both of the SPEED UP control switches may be ON to provide speed up factors of 20, 60 or 1200 times normal.

After the Sequencer Breadboard has been cleared and before the INHIBIT is released, the update operation may take place. The 7 HOUR output toggle flip-flop indicators are used to monitor the update operation. The UPDATE ENABLE switch must be ON; otherwise, the update pulses will be counted as normal 1 MINUTE inputs and the entire Launch Counter will be affected. The first pulse generated by the UPDATE push button should generate a 7 HOUR output and therefore change the state of the output

indicator from OFF to ON. The divide by 7 ring in the Launch Counter then advances one position for each update pulse; this should generate a 7 HOUR output for every 7 input pulses and cause the output indicator to change state. The final position of the divide by 7 ring is determined by the number of input pulses in excess of exact multiples of 7. Each update pulse should also result in an UPDATE VERIFY output which will cause the UPDATE VERIFY indicator to change state. If the Sequencer has been cleared before the update operation, the update input pulses should have no other effect than to cause the 7 HOUR outputs and provide the UPDATE VERIFY output.

The COUNT INHIBIT may be released from each replica individually by turning OFF separate COUNT INHIBIT switches or from all replicas simultaneously by turning ON the INHIBIT RELEASE switch. If each replica is released individually, the starting time is the time at which the second COUNT INHIBIT switch is switched OFF. Individual switching of the COUNT INHIBIT switches is normally expected to cause differences on the 1 SECOND output due to lack of initial synchronism.

Sequencer operation after the release of COUNT INHIBIT should be as follows:

The 1 MINUTE output indicators will immediately (within one-twentieth of a second) change from OFF to ON. The 7 HOUR output indicator will change state once for every  $7 \times 60 = 420$  minutes, with the timing of the first output dependent upon the initial state of the divide by 7 ring as determined by the update operation. The L-1 relay will be set after 56 minutes and set pulses will occur again every 68 minutes. Likewise, the L-2

relay will be set after 60 minutes and set pulses will occur every 60 minutes thereafter. The L-3 relay will be set after  $60 \times 17 = 1020$  minutes and set pulses will occur every 1020 thereafter. However, the setting of L-3 will set both L-1 and L-2 (if not already set) and inhibit any further set pulses to them.

## 6.2 Single Rank Testing

The purpose of the voter difference detectors is to monitor the voter outputs to verify that all voters in the same "file", or location, always provide the same logical output. Proper operation of the voter difference detectors (and voter forcing switches) is verified by applying all possible combinations of inputs to the voter difference detectors (using the voter forcing switches) and observing that there is a voter difference indication whenever the inputs are not all alike.

There are several procedures that may be used to provide all 8 combinations of 3 inputs to the voter difference detectors. Perhaps the simplest procedure for manipulating the switches is as follows:

- 1.) With the VOTER LATCH switched off, switch all voter forcing switches to the "0" state. All voter indicators should remain OFF. Individually switch each forcing switch to the "1" state and return to the "0" state. Observe that all voter indicators should remain ON while each of the switches is switched to "1" and should go OFF after returning each switch to the "0" state.

- 2.) Switch all voter forcing switches to the "1" state. All voter indicators should remain OFF. Repeat the procedure described above,

moving each switch from "1" to "0" and returning to "1".

The voter difference detector tests are intended to verify that the voter difference detectors and their forcing switches are operating. However, the probability is high that even if a voter difference detector does not indicate a failure in normal operation, that failure will still be detected by processor difference detectors. Therefore, it is not expected that these tests would be conducted frequently. It should also be noted that the system is rendered inoperative by the complete test procedure described above. If it is desired to leave the system operative as much as possible, only one or two voter forcing switches should be applied at a time (with opposite states when two switches are operated). The system can then be operated dynamically on the remaining line (or lines). If operation is attempted while using the voter forcing switches, the processor difference detectors will also indicate differences.

The purpose of the processor difference detectors is to provide a continuous monitor of the processor outputs to majority voters. The operation of both the processor forcing switches and the processor difference detectors may be verified by the singular rank testing procedure as outlined below, or in exactly the same manner as the voter forcing switches and voter difference detectors as outlined above.

The processor difference detectors normally indicate all logic errors generated at the processor outputs to majority voters. However, singular rank testing is necessary to verify that each non-redundant replica can actually operate independently, with the other replicas disabled, and that the voters are capable of transmitting correct signals under these conditions.

conditions. If the voter difference detectors are monitored during singular rank testing, it can be verified that the voters all provide the same majority output for all possible inputs. Singular rank testing is intended for use in an operating system, with proper system operation throughout the tests.

The singular rank testing procedure is summarized as follows:

- 1.) The system is operated in all normal functional modes. If the difference detectors indicate that there are logic errors present, they should be repaired; otherwise the system will fail during the singular rank tests.

- 2.) One rank is chosen as the normally operating non-redundant system. Its processor forcing switch must be left in the normal non-forcing mode. One of the remaining forcing switches is switched to the "0" state, the other to the "1" state. The processor difference detectors are observed to verify that the use of any two forcing switches in opposite states causes the indicators to be ON. (If the system is operating with outputs of both "1's" and "0's" to voters, the use of any one forcing switch should cause a difference indication.) If all of the detectors indicate processor differences for all the combinations of forcing inputs, then it is verified that all processor detectors and forcing switches are operative.

- 3.) The system is operated to verify that the rank chosen for normal operation is capable of correct operation for the desired conditions. If it is desired to further check for the possibility of unknown coupling

between ranks (other than at the voters), the states of the two remaining forcing switches may be reversed and the operational test repeated.

4.) The procedure described above is essentially repeated for the remaining replicas. The replica formerly forced to the "0" state is now switched to the normal mode, the other forcing switch is reversed from the "1" state to the "0" state, and the switch previously in the normal mode is switched to the "1" state. Operation of the detectors and system functional capability is verified as before.

5.) The procedure is repeated again, with the last replica (previously forced to the "0" state) now switched to normal mode, the other forcing switch reversed, and the switch previously in the normal mode switched to the "1" state. Operation is verified as before.

The proper operation of elements throughout the system verifies that all processors are operating correctly and that the voters are capable of transmitting correct signals. In addition, if there is no voter difference indication during the procedure described above, then the voters provide the majority output for all possible inputs.

The difference detectors may be operated in two modes, either continuous indication or display latch. When the indicator latch switch is ON, any output from the difference detector will cause the indicator to latch and remain ON; when the indicator latch switch is OFF, the indicator provides a continuous display of the difference detector output. Separate indicator control switches are provided for the voter and processor detectors. It is expected that the voter detectors would be operated with the indicator latch ON except during the voter detector testing procedure. The processor

detectors should be operated with the indicator latch OFF during the singular rank testing procedure; whether the indicator latch should be ON during normal operation depends upon the sensitivity of the detector and the alignment of the output pulses from the processors because it is possible for these outputs to vary in phase without actually being in error.

#### 7. LOGIC DIAGRAMS, SCHEMATICS AND PARTS LISTS

The following pages contain complete documentation of all the circuitry which will be in the system.

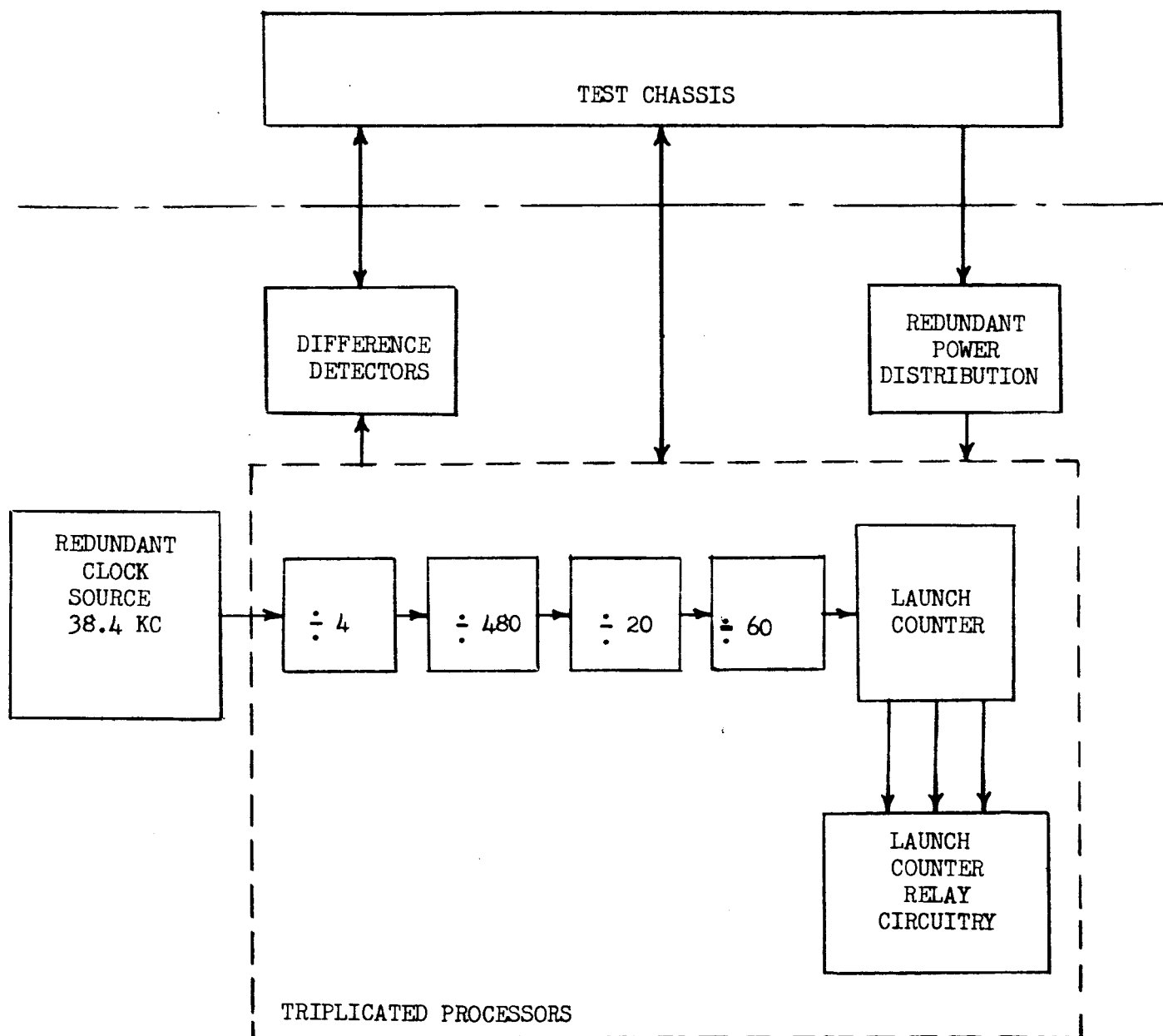
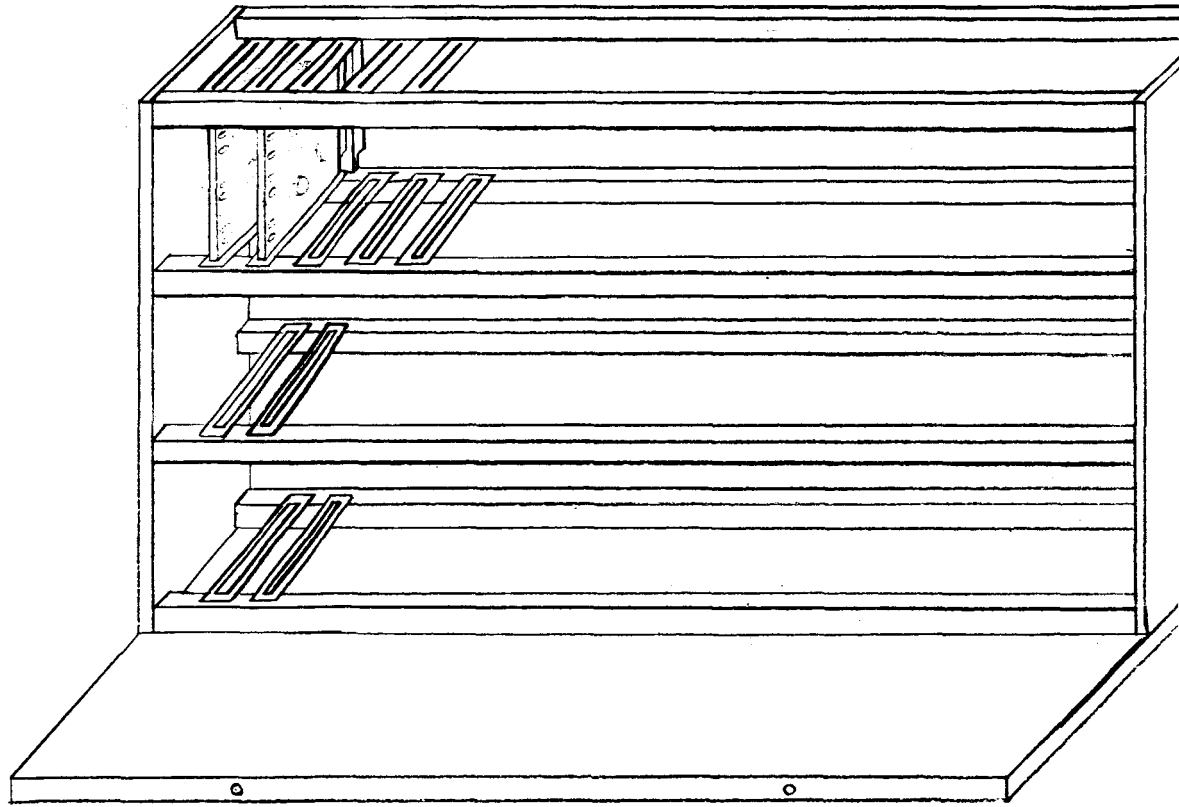
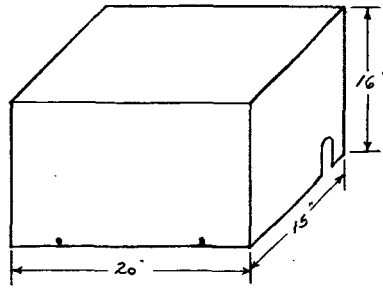
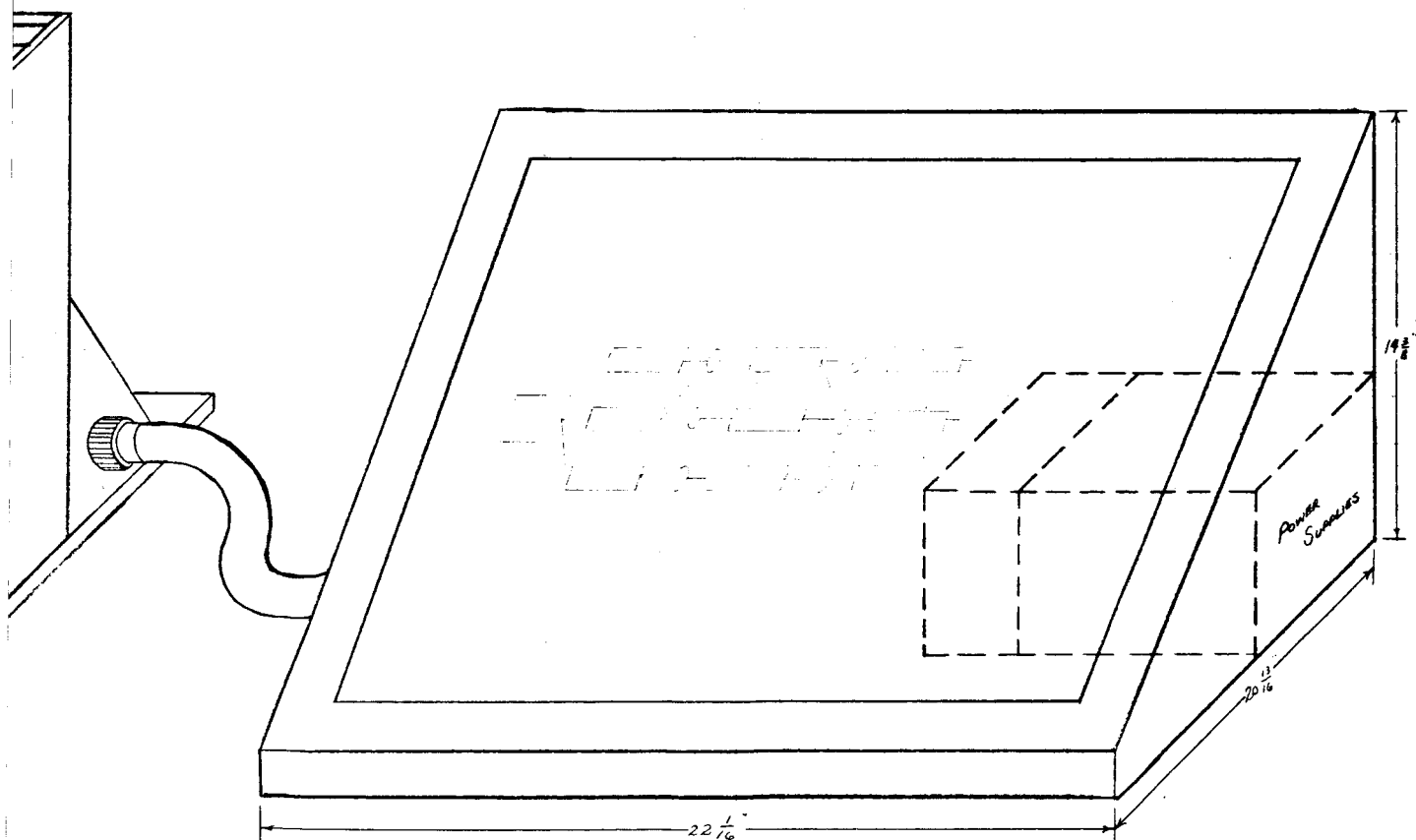


Figure 7-1. Block Diagram, Redundant Sequencer Breadboard





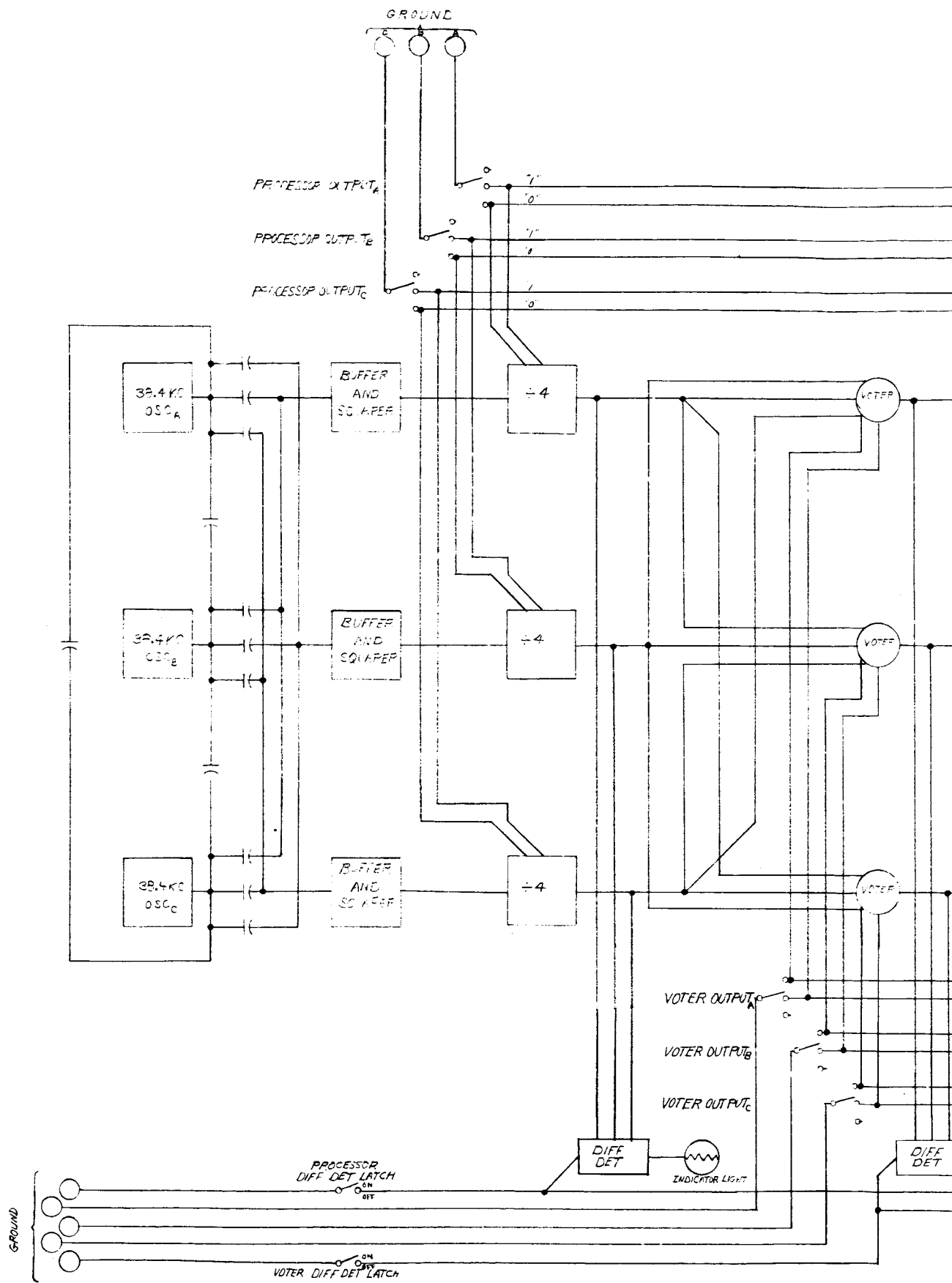
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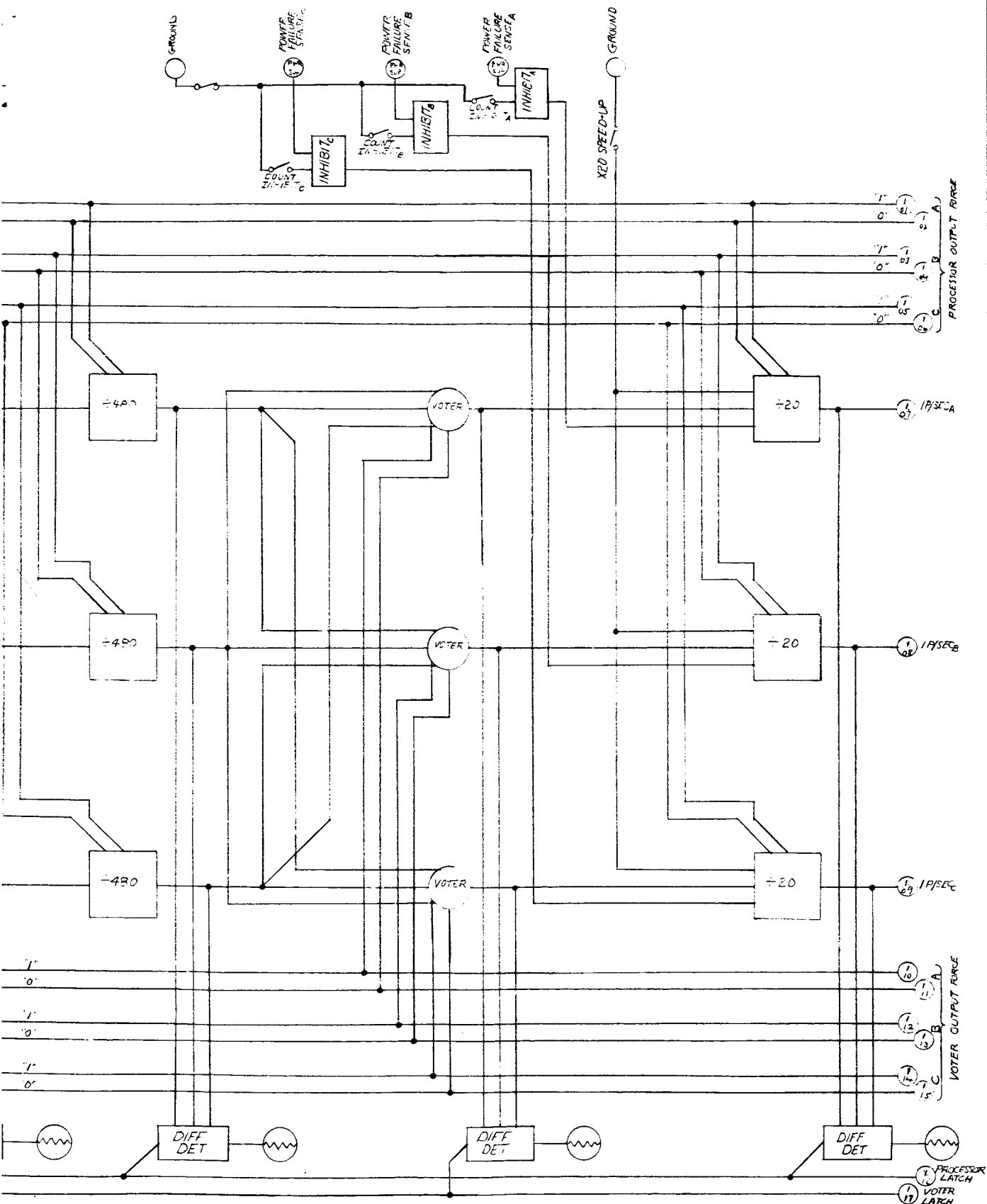
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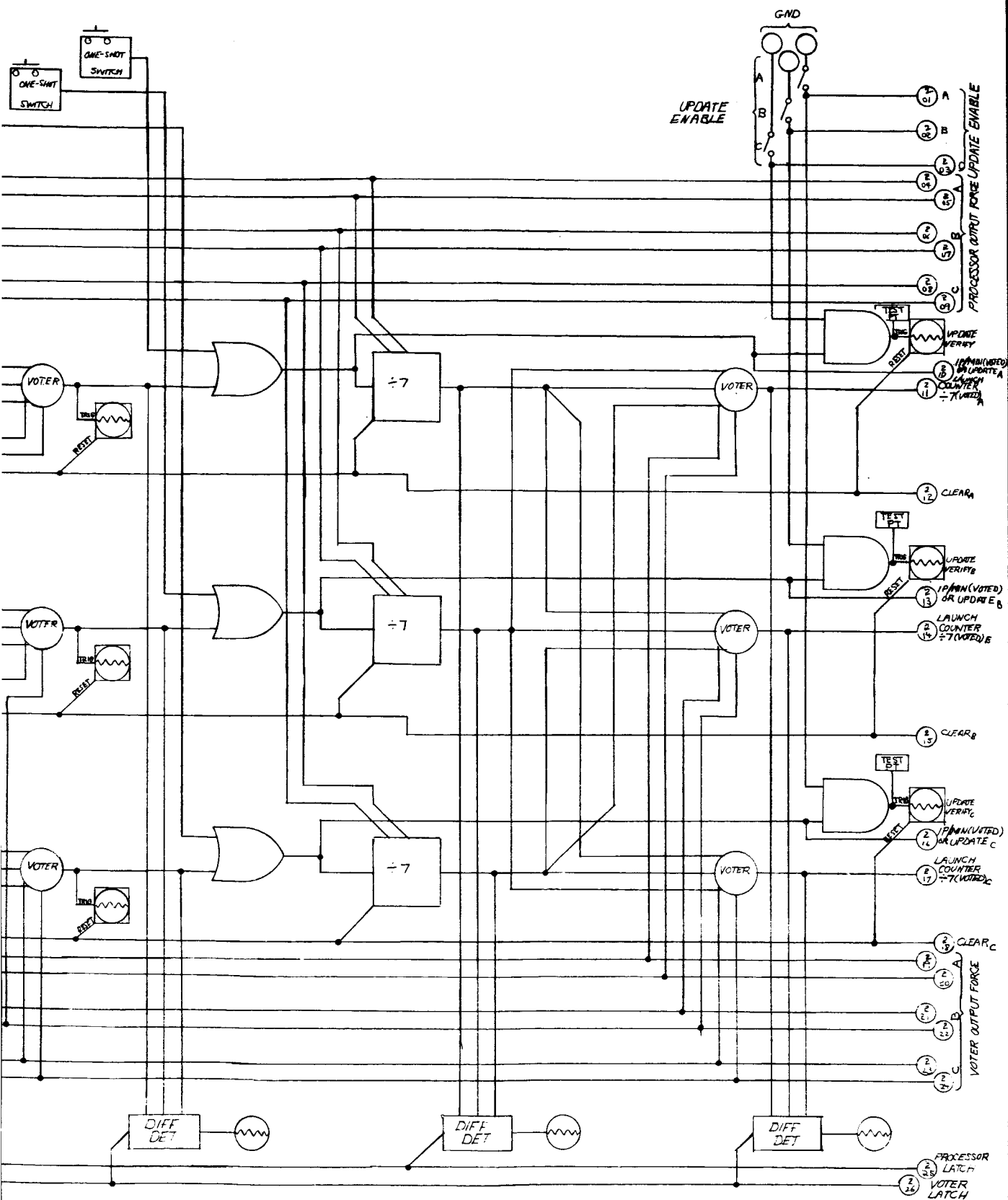




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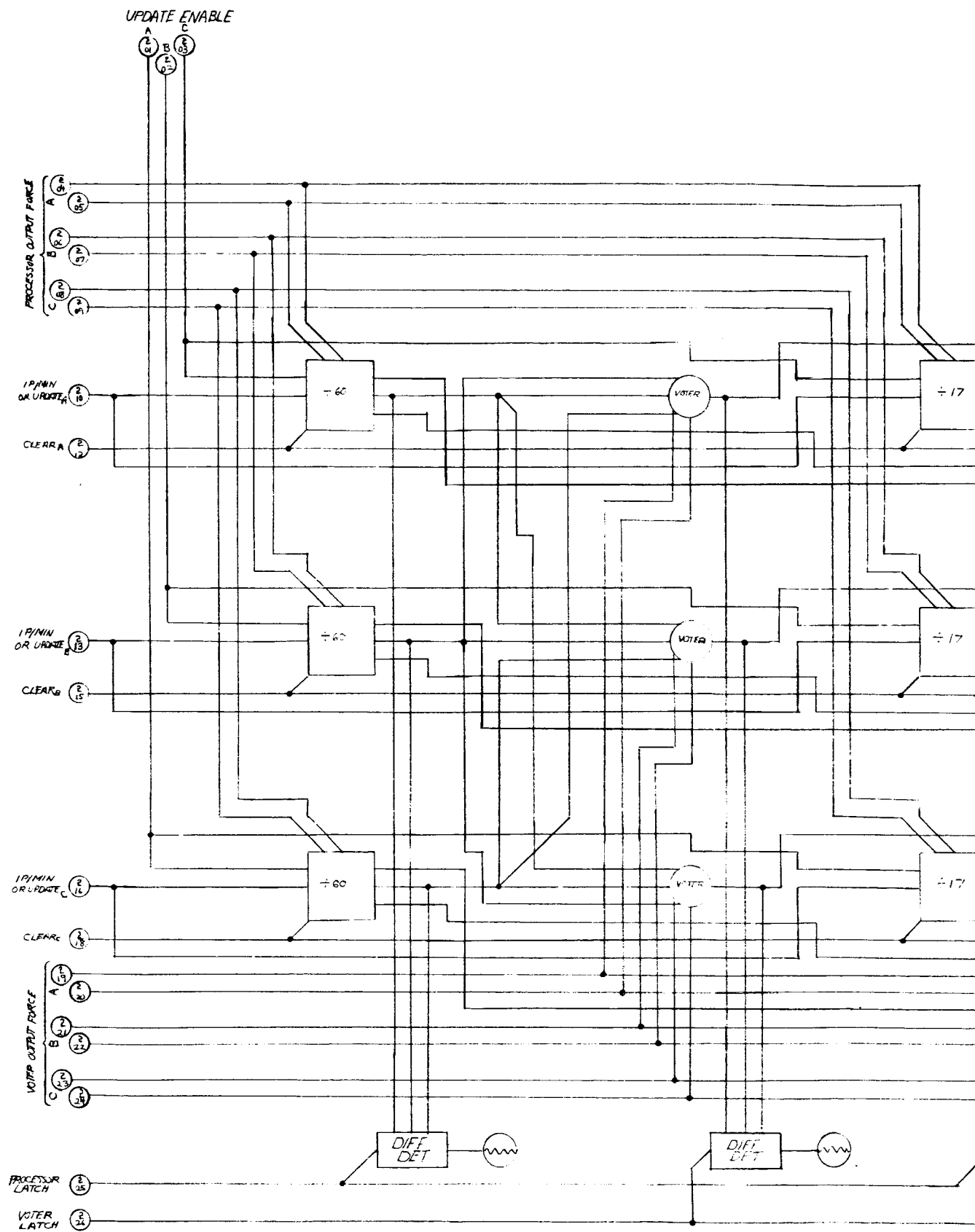
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	FIG. 7-4/1	SHEET 1 OF 4 SHEETS



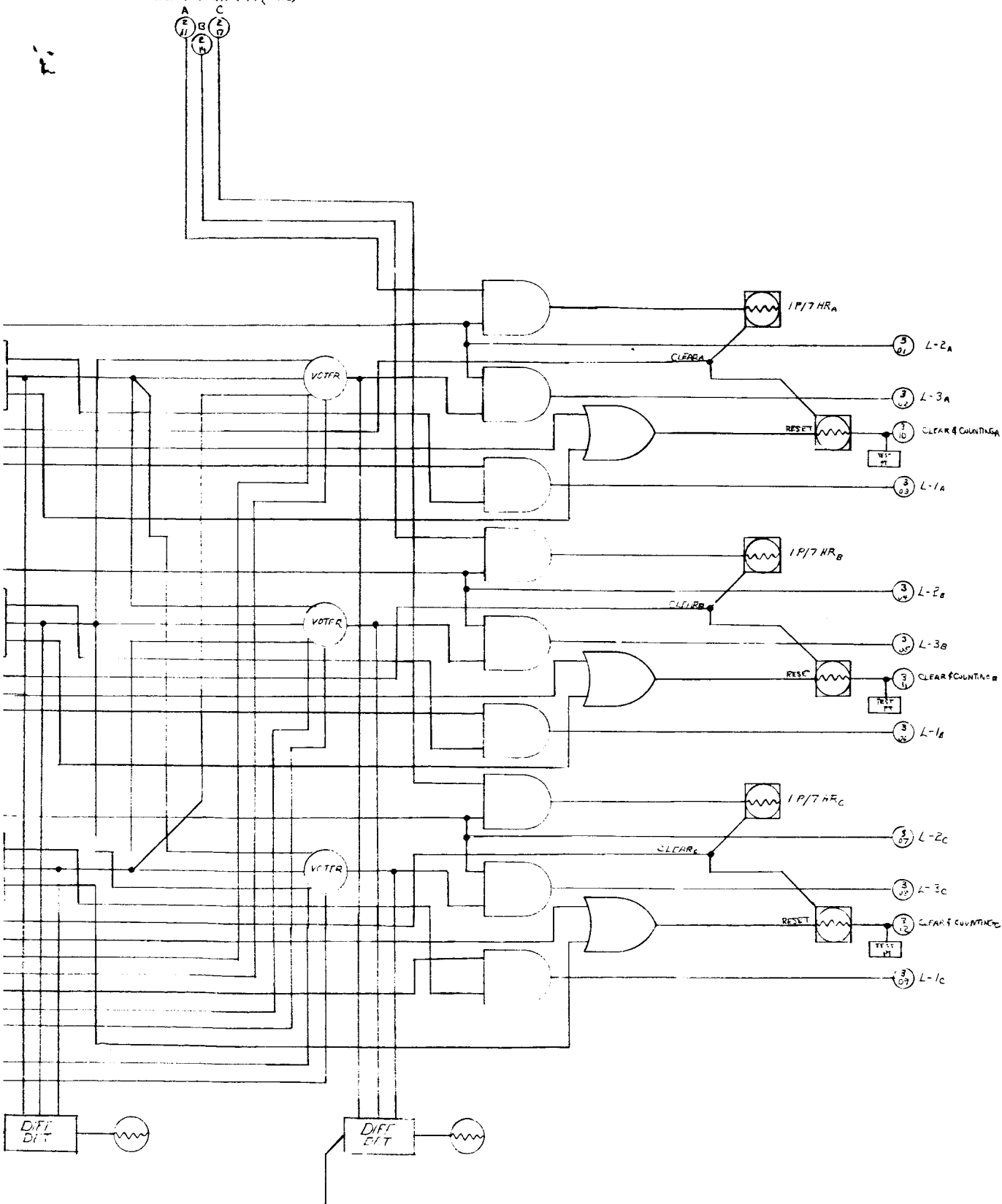


7

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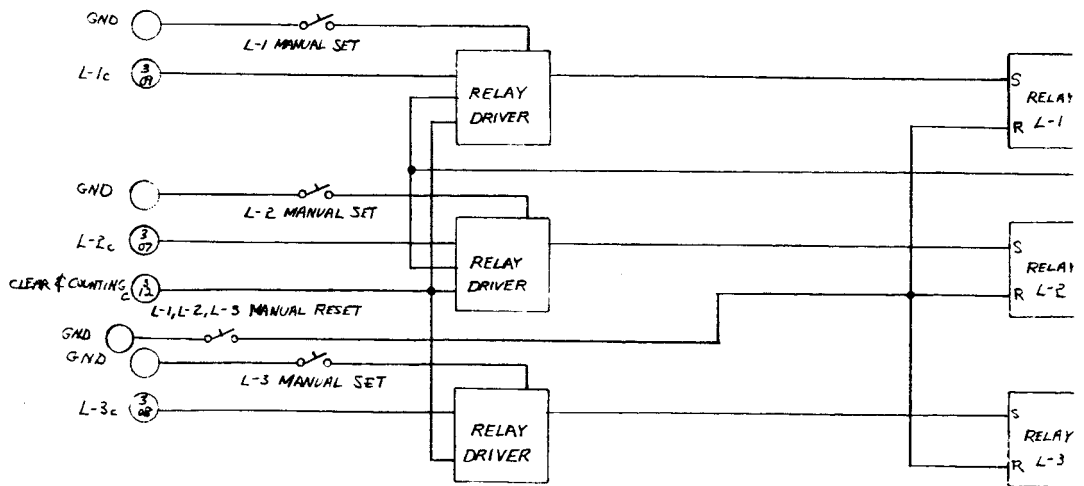
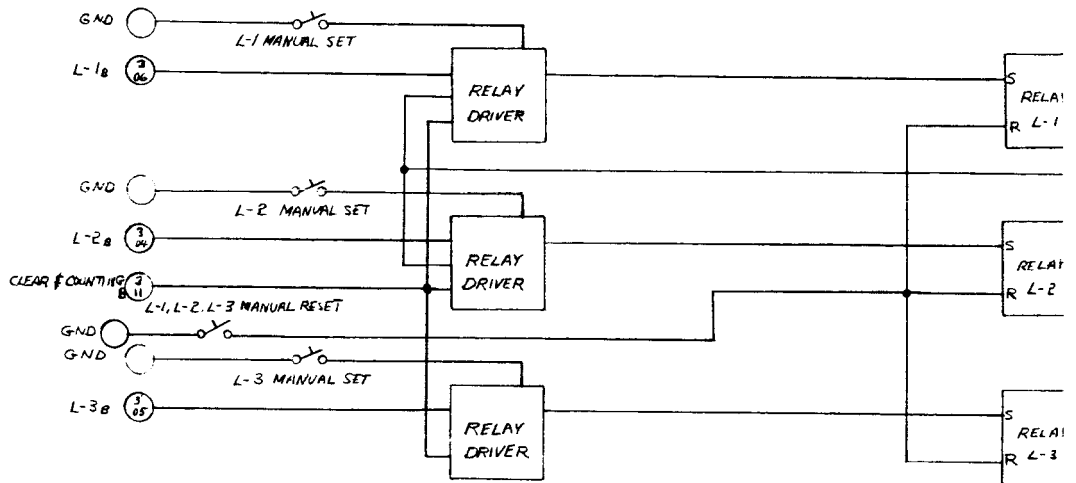
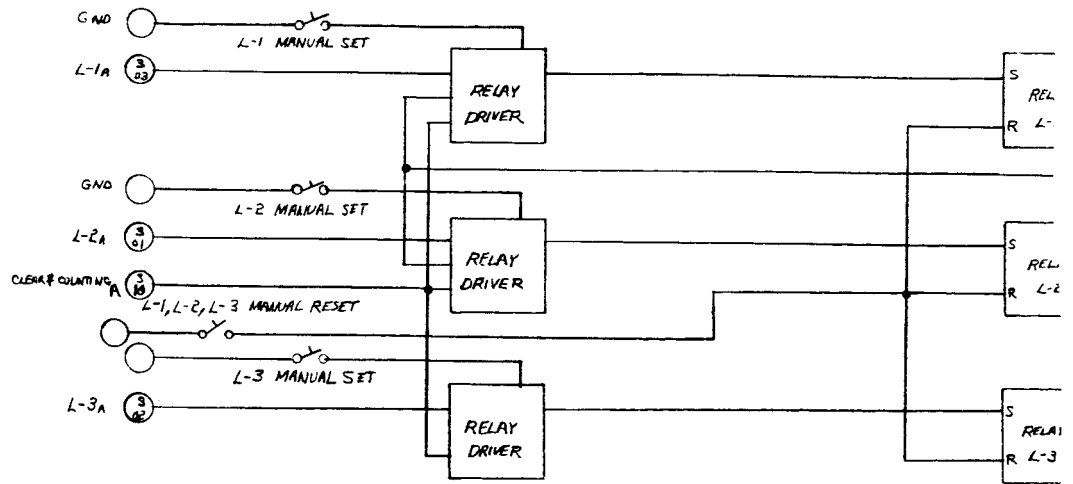


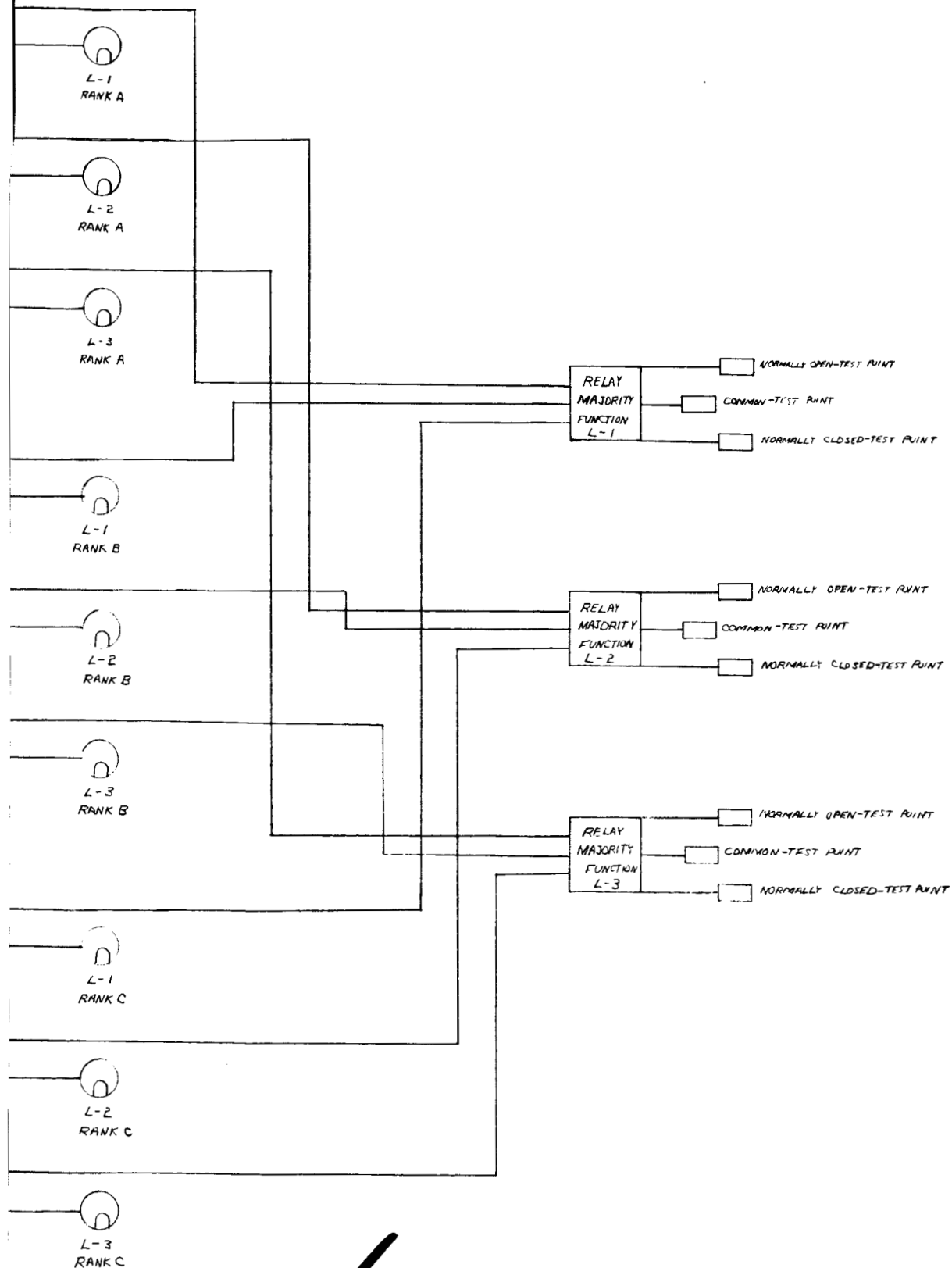
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2

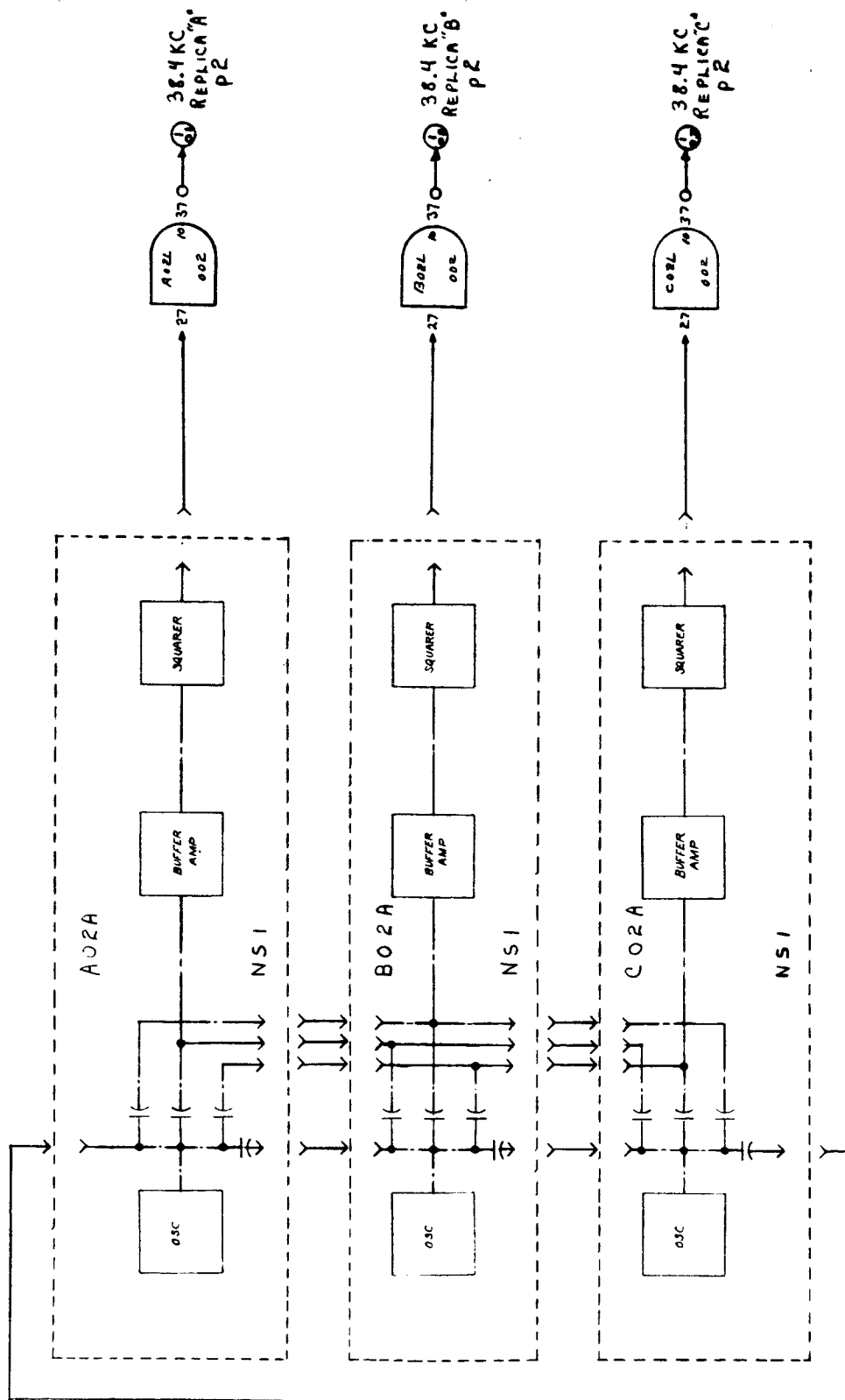
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	<i>FIG. 7-4/3</i>	SHEET 3 OF 4 SHEETS





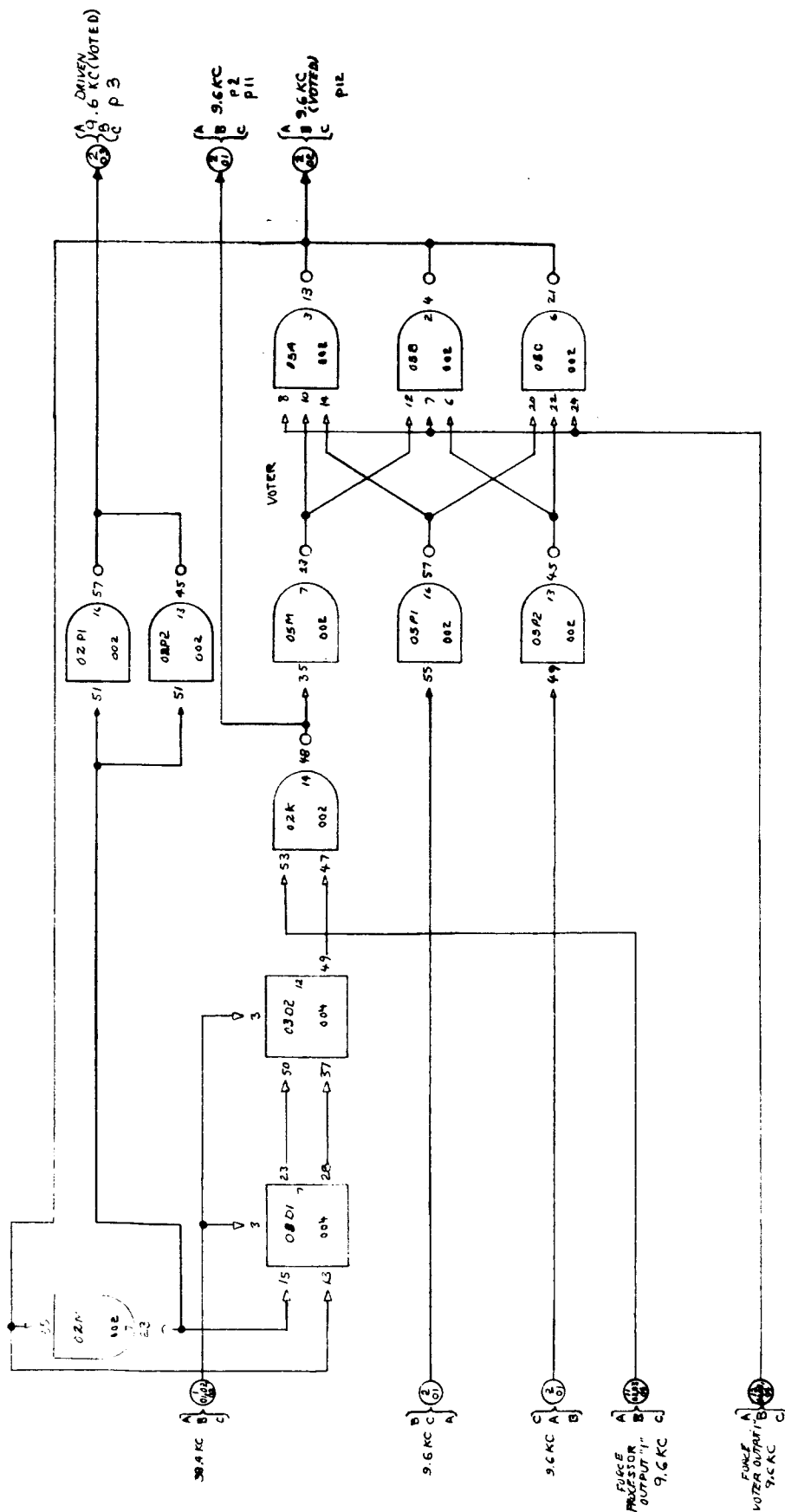
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	FIG. 7-4/4	NUMBER TO BE APPROVED TO FINAL DRAWING SK <i>C</i>
	SHEET 4 OF 4 SHEETS	



REVISIONS

DESIGNED APPROVED CHARGE	ENGINEERING SKETCH	WESTINGHOUSE ELECTRIC CORPORATION SURFACE DIVISION BALTIMORE, MD., U. S. A. NUMBER TO BE ADDED TO FINAL DRAWING <b>SK B</b>
	TITLE	
	REDUNDANT CLOCK SOURCE FIG. 7-5	
SHEET 1 OF 14 SHEETS		



DESIGNED APPROVED CHANGED	ENGINEERING SKETCH	WESTINGHOUSE ELECTRIC CORPORATION SURFACE DIVISION BALTIMORE, MD., U. S. A. NUMBER TO BE ASSIGNED TO FINAL DRAWING SK B SHEET 2 OF 14 SHEETS
	TITLE DIVIDE-BY-4 COUNTER	
	FIG. 7-6	

11/11 A  
B  
C

11/11 A  
B  
C

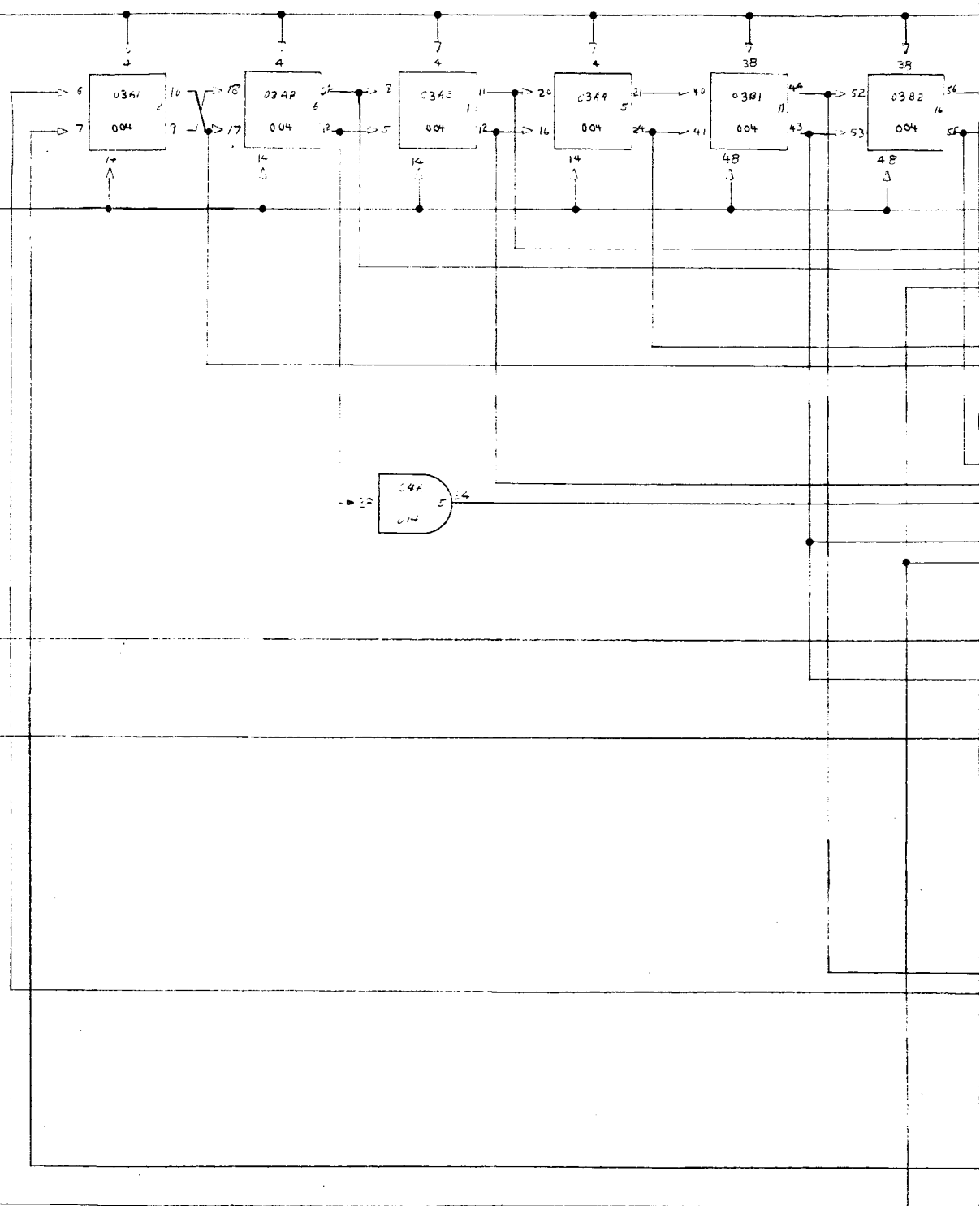
20 P/SEC  
A  
B  
C

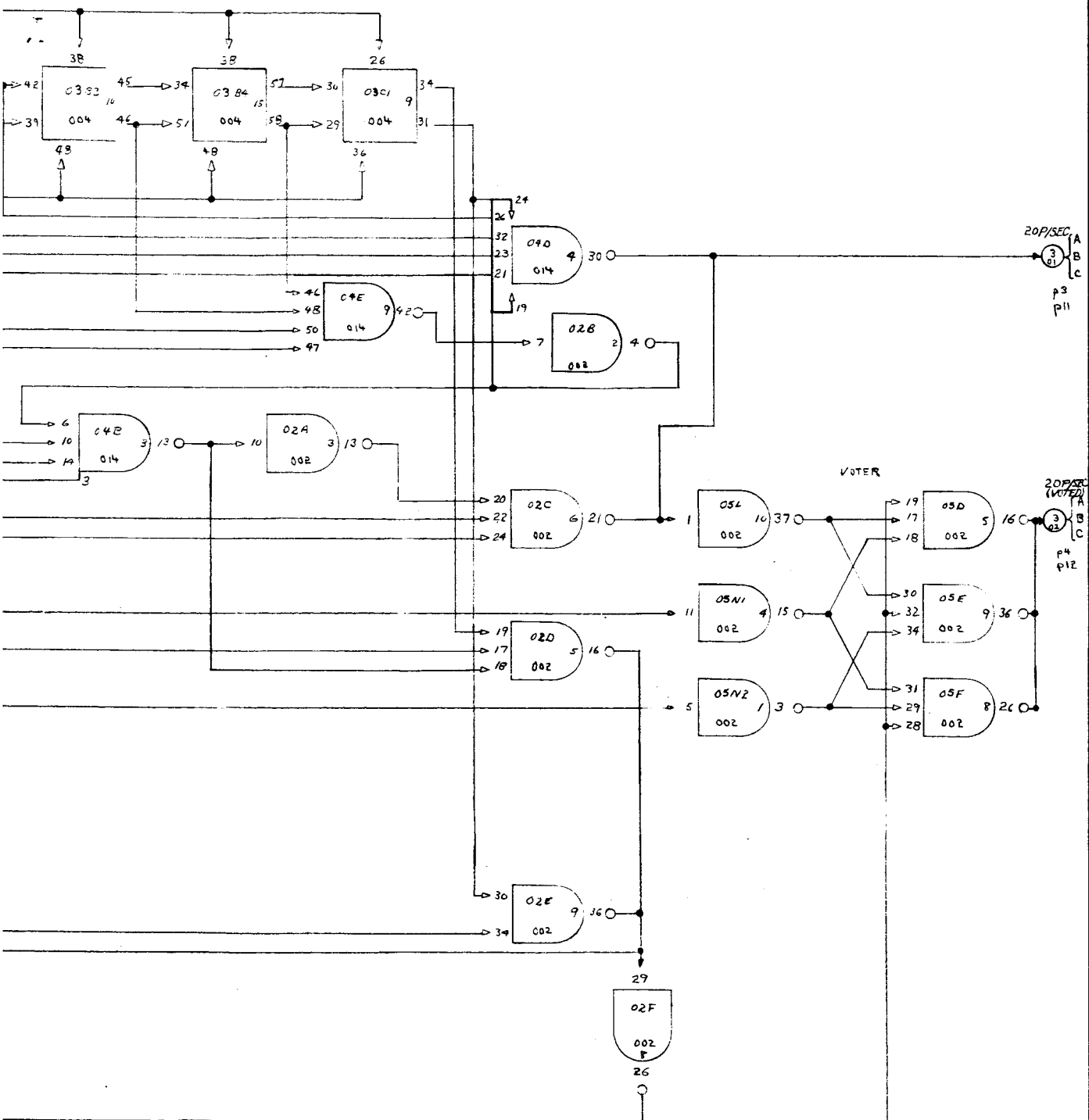
20 P/SEC  
A  
B  
C

20 P/SEC  
A  
B  
C

20 P/SEC  
A  
B  
C

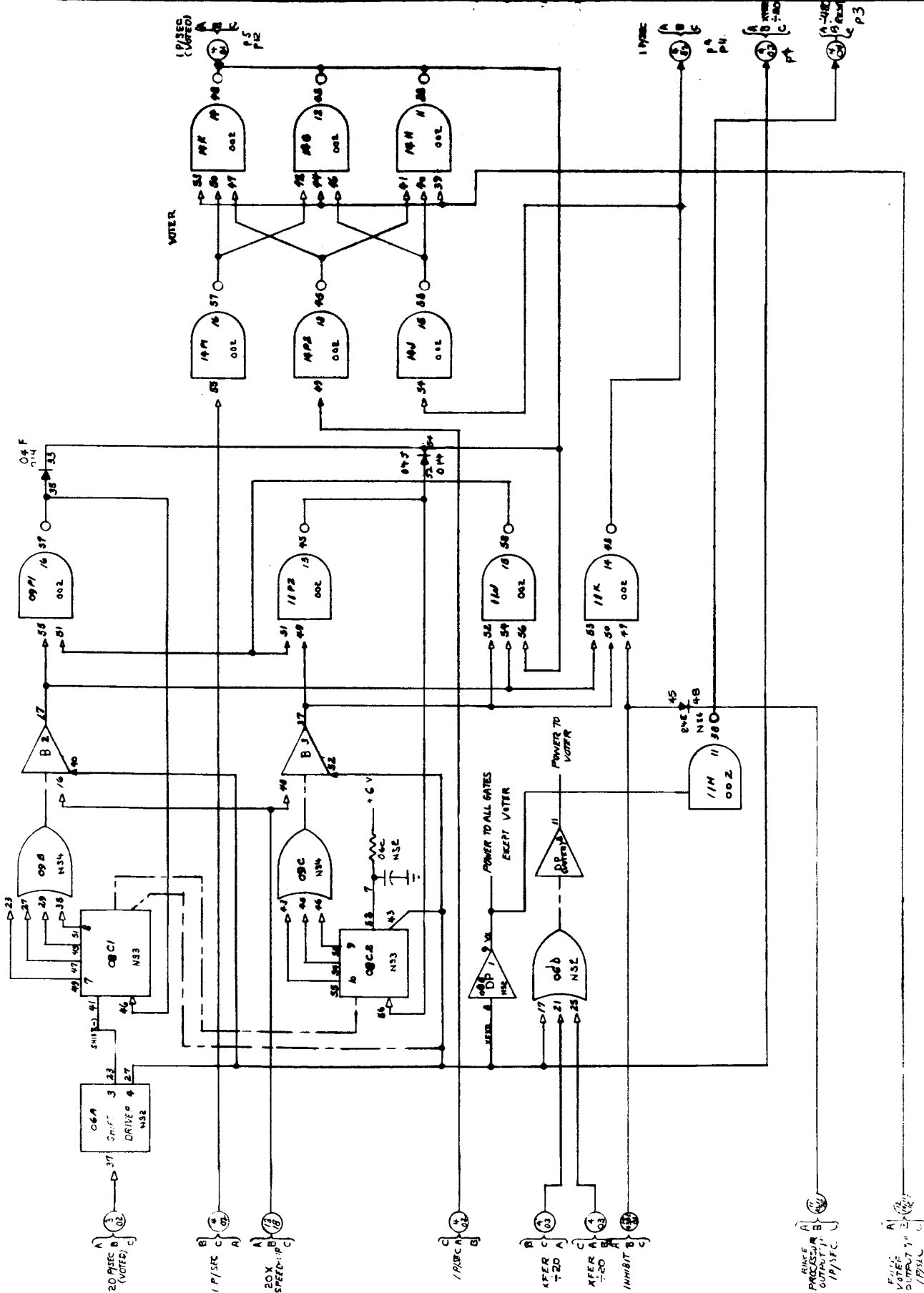
REVISIONS

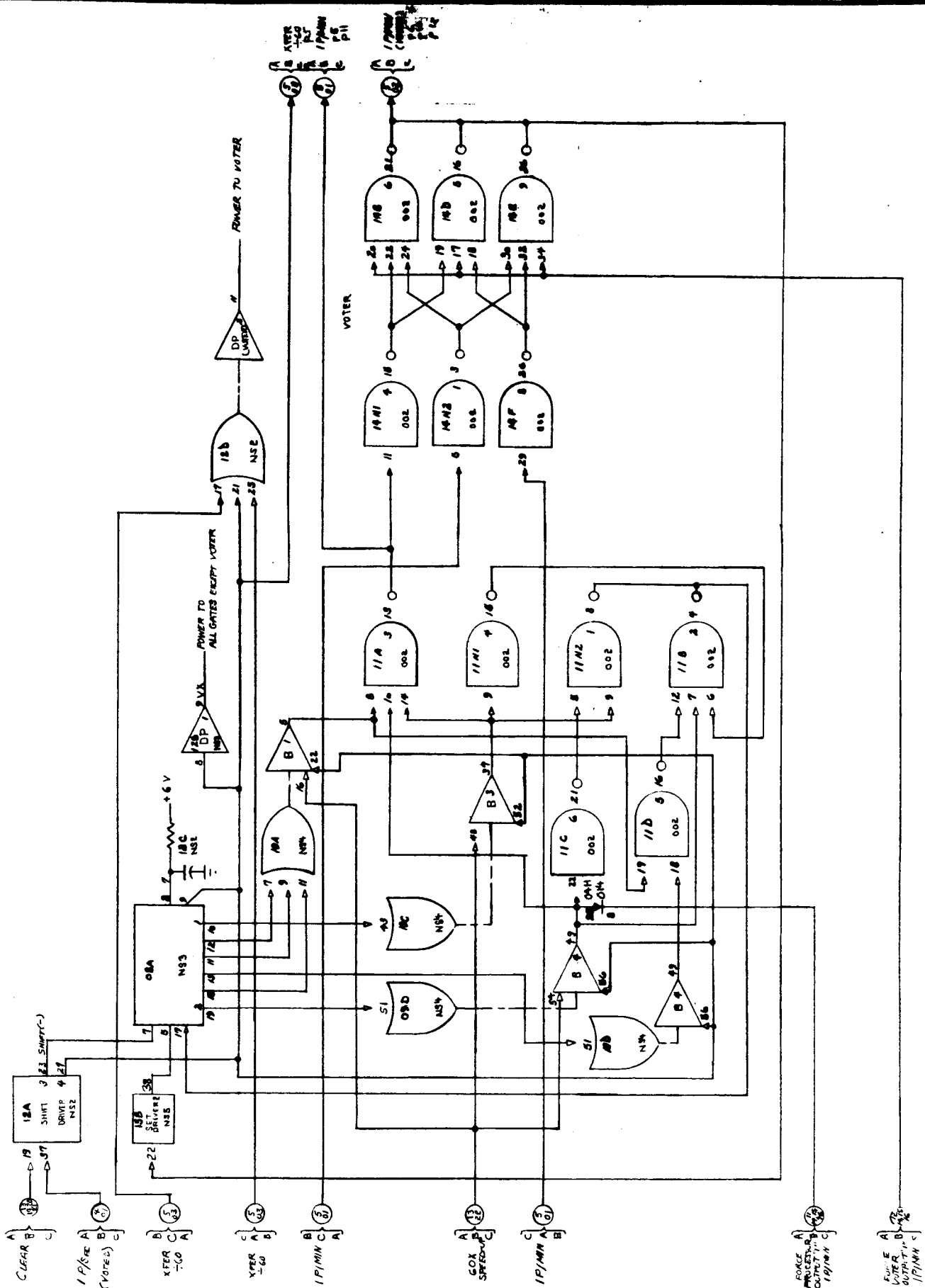




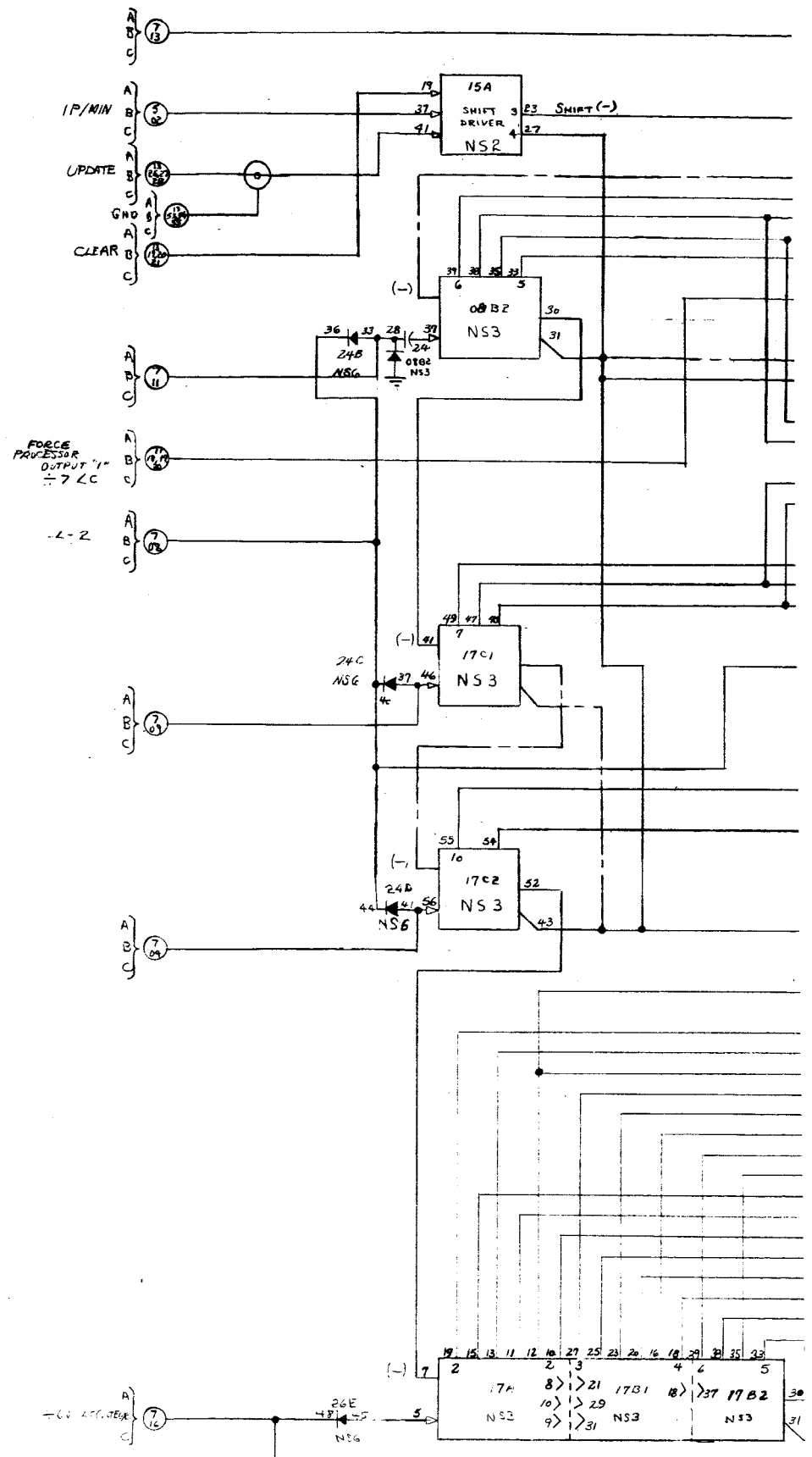
*V*

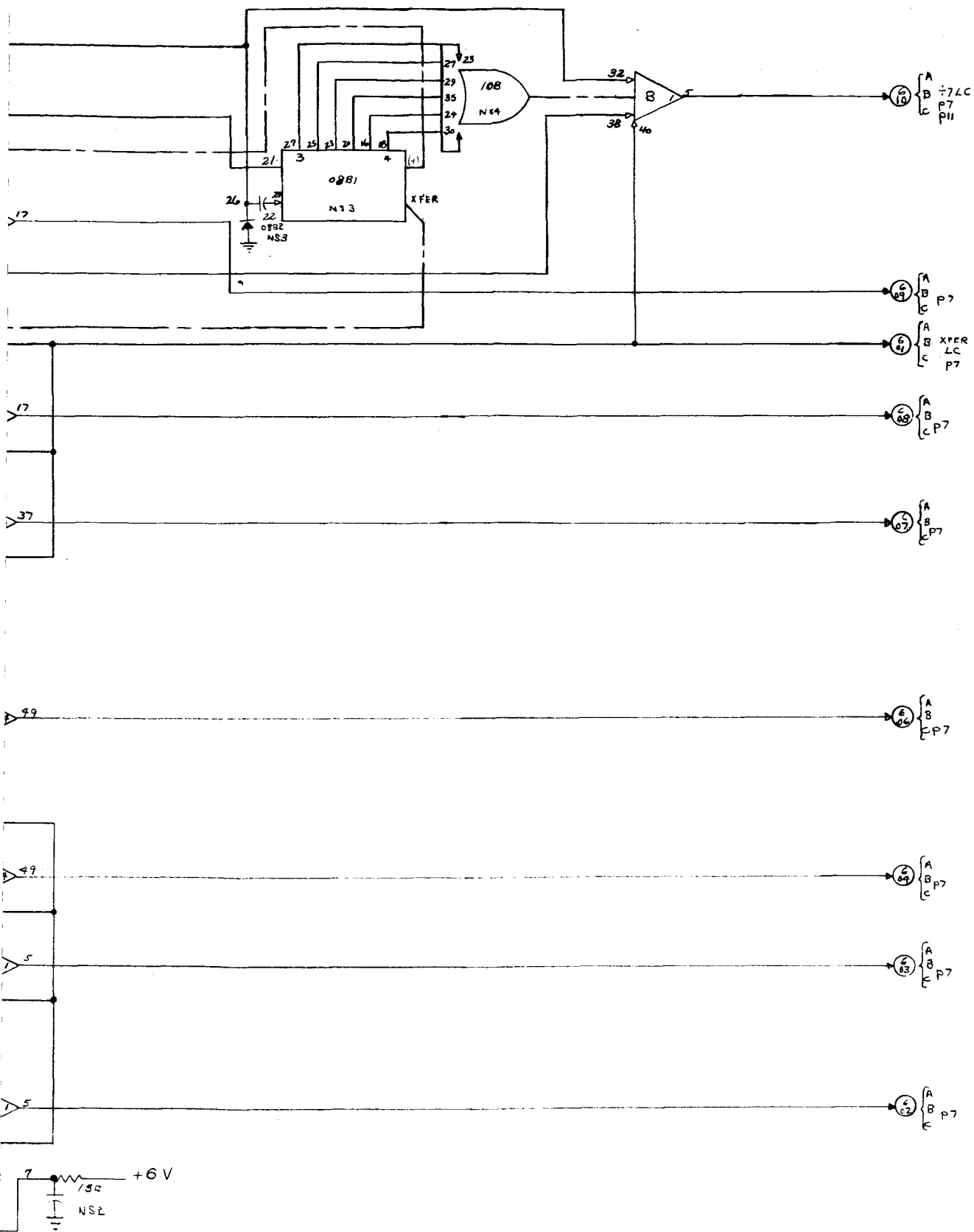
DES. APPROVED. CHANGE	ENGINEERING SKETCH	WESTINGHOUSE ELECTRIC CORPORATION SURFACE DIVISION BALTIMORE, MD., U. S. A. SK C SHEET 3 OF 14 SHEETS
	TITLE	
	DIVIDE-BY-480 COUNTER FIG. 7-7	





DATE _____ APPROVED _____ CHARGE _____	TITLE <div style="text-align: center; font-size: 1.5em;"> <i>DIVIDE-BY-60 COUNTER</i> </div>	WESTINGHOUSE ELECTRIC CORPORATION SURFACE DIVISION BALTIMORE, MD., U. S. A.
		SKETCHED TO BE APPROVED TO FINAL DRAWING <div style="display: flex; justify-content: space-around; font-size: 1.5em;"> <span>SK</span> <span>B</span> </div>
	<div style="text-align: center; font-size: 1.5em;"> <i>FIG. 7-9</i> </div>	SHEET 5 OF 14 SHEETS

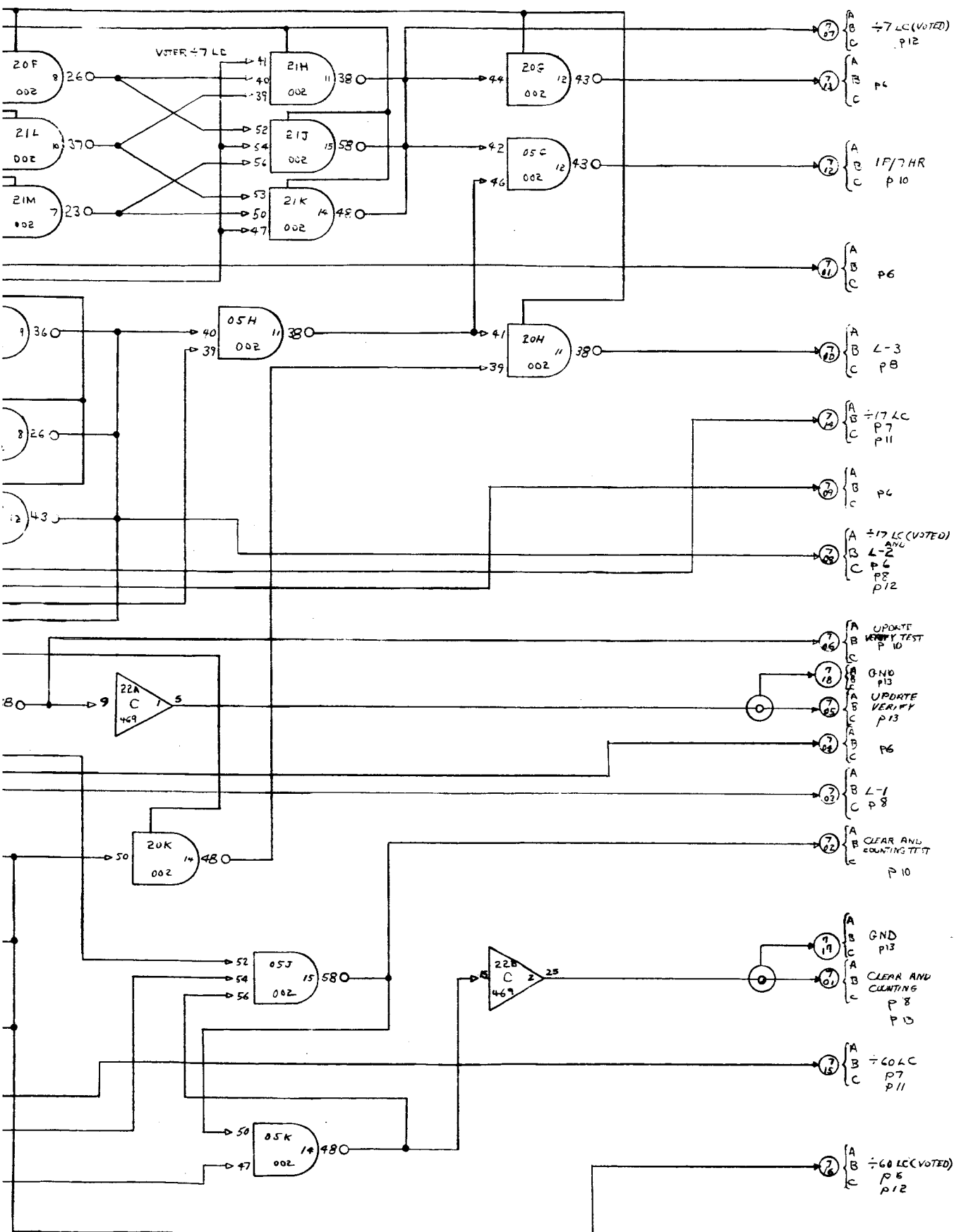




✓

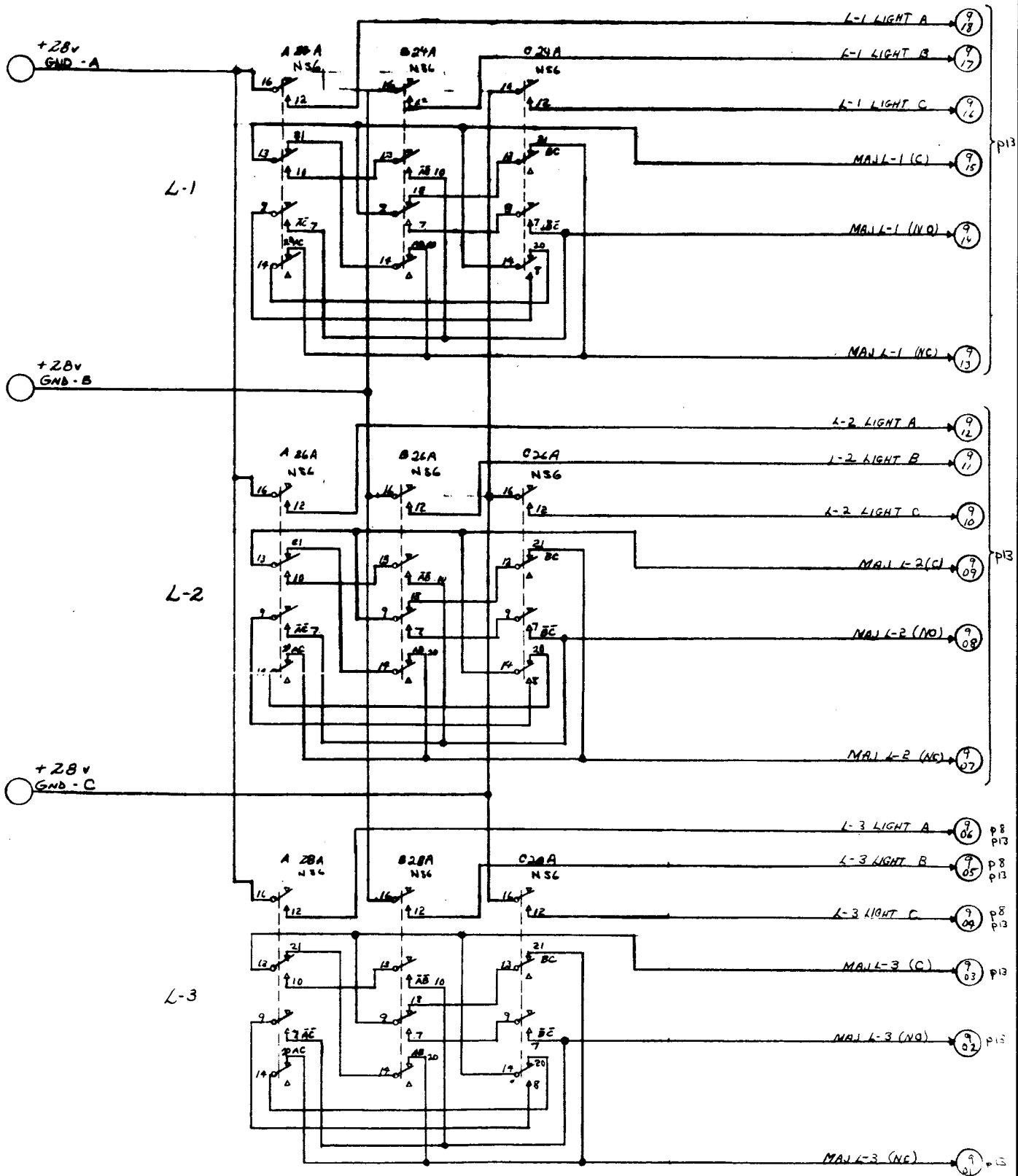
ENG. _____ APPROVED _____ CHARGE _____	ENGINEERING SKETCH	<b>WESTINGHOUSE ELECTRIC CORPORATION</b> SURFACE DIVISION BALTIMORE, MD., U. S. A. NUMBER TO BE ASSIGNED TO FINAL DRAWING <b>SK C</b> SHEET 6 OF 14 SHEETS
	TITLE	
	LAUNCH COUNTER REGISTERS AND BUFFERS	
	FIG. 7-10/1	





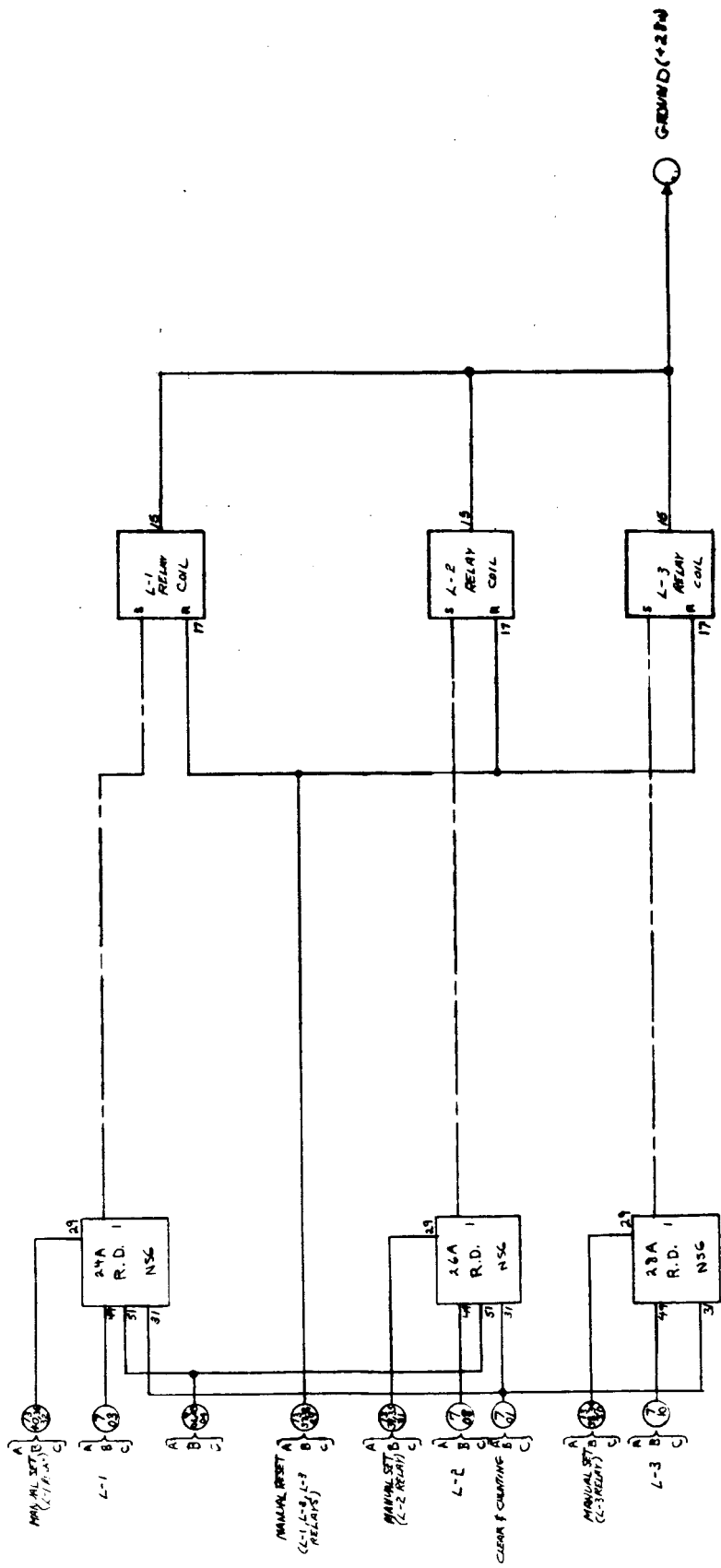
2

ENGINEERING SKETCH		<b>WESTINGHOUSE ELECTRIC CORPORATION</b> SURFACE DIVISION BALTIMORE, MD., U. S. A. SK C SHEET 7 OF 14 SHEETS
DATE	TITLE	
APPROVED	LAUNCH COUNTER DECODE AND VOTERS	
CHANGE	FIG. 7-10/2	



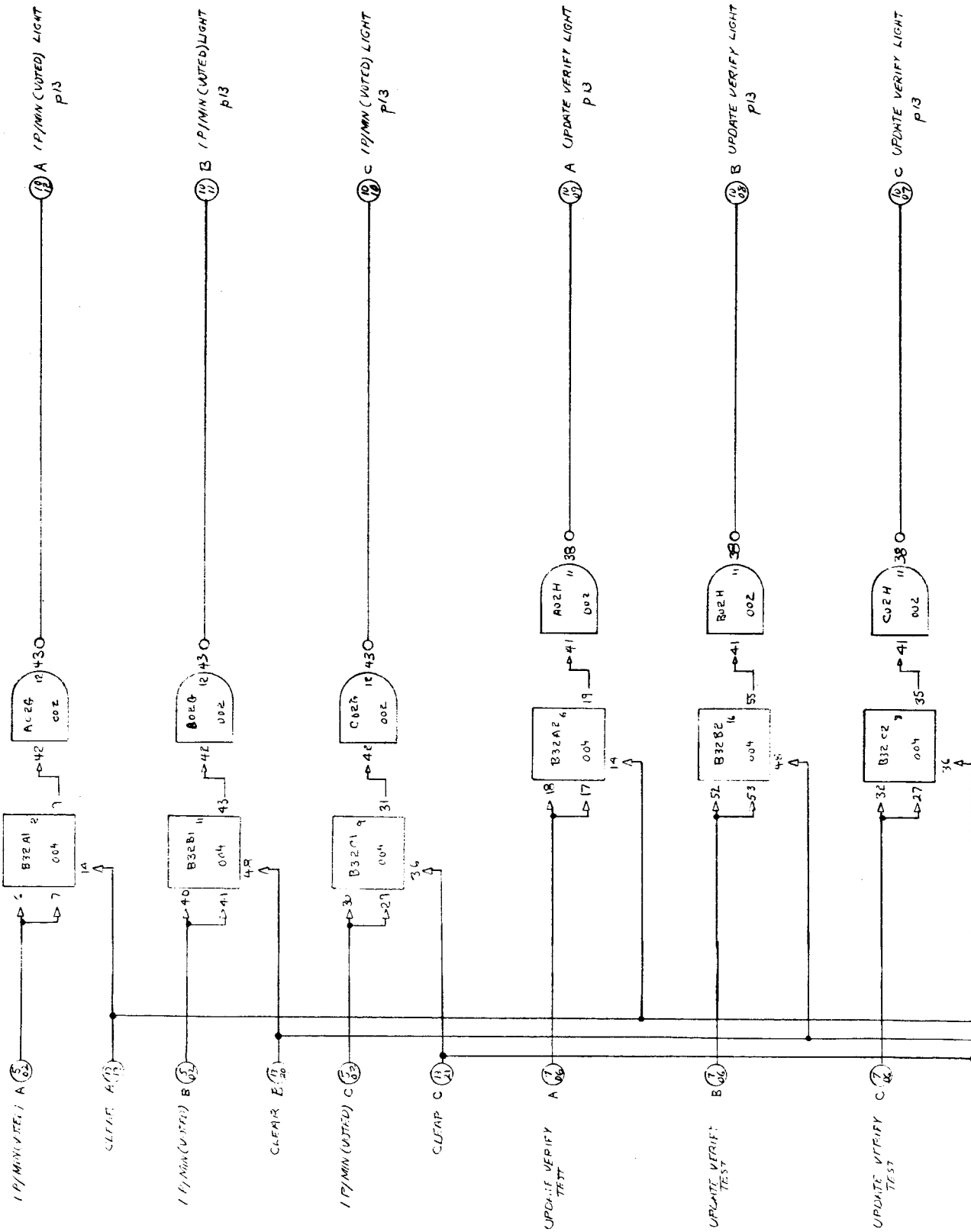
DESIGNED APPROVED CHARGE	ENGINEERING SKETCH		WESTINGHOUSE ELECTRIC CORPORATION ELECTRONICS DIVISION BALTIMORE, MD., U. S. A. SK B SHEET 9 OF 12 SHEETS
	TITLE		
	LAUNCH COUNTER RELAY CIRCUITRY RELAY CONTACT WIRING FIG. 7-11/1		
	APPROVED TO BE SUBMITTED TO FINAL DRAWING		

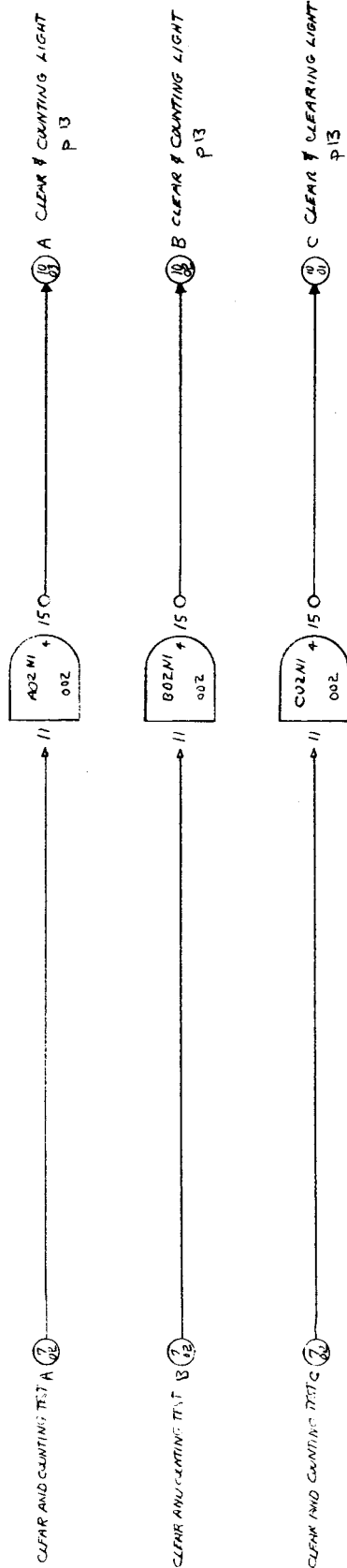
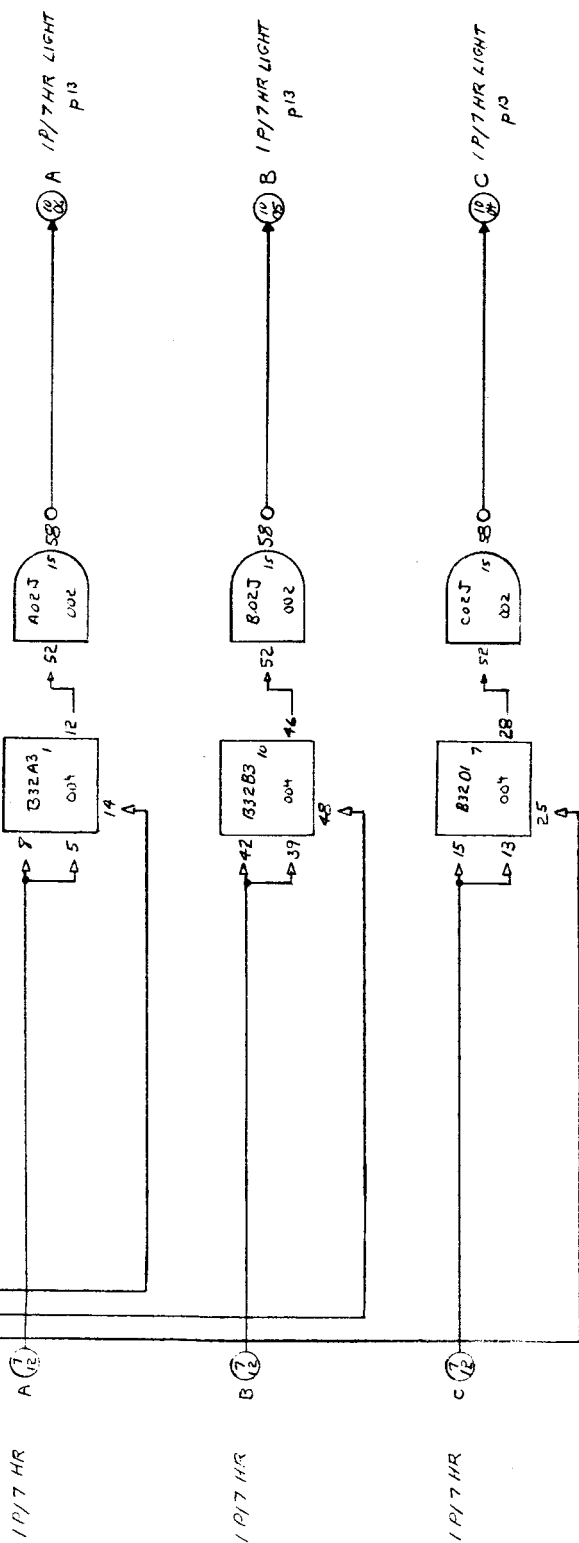
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ENGINEERING SKETCH		WESTINGHOUSE ELECTRIC CORPORATION SURFACE DIVISION BALTIMORE, MD., U. S. A.	
TITLE LAUNCH COUNTER RELAY CIRCUITRY		DRAWN TO BE ASSIGNED TO FINAL DRAWING	
RELAY COIL WIRING		SK B	
FIG. 7-11/2		SHEET 8 OF 14 SHEETS	

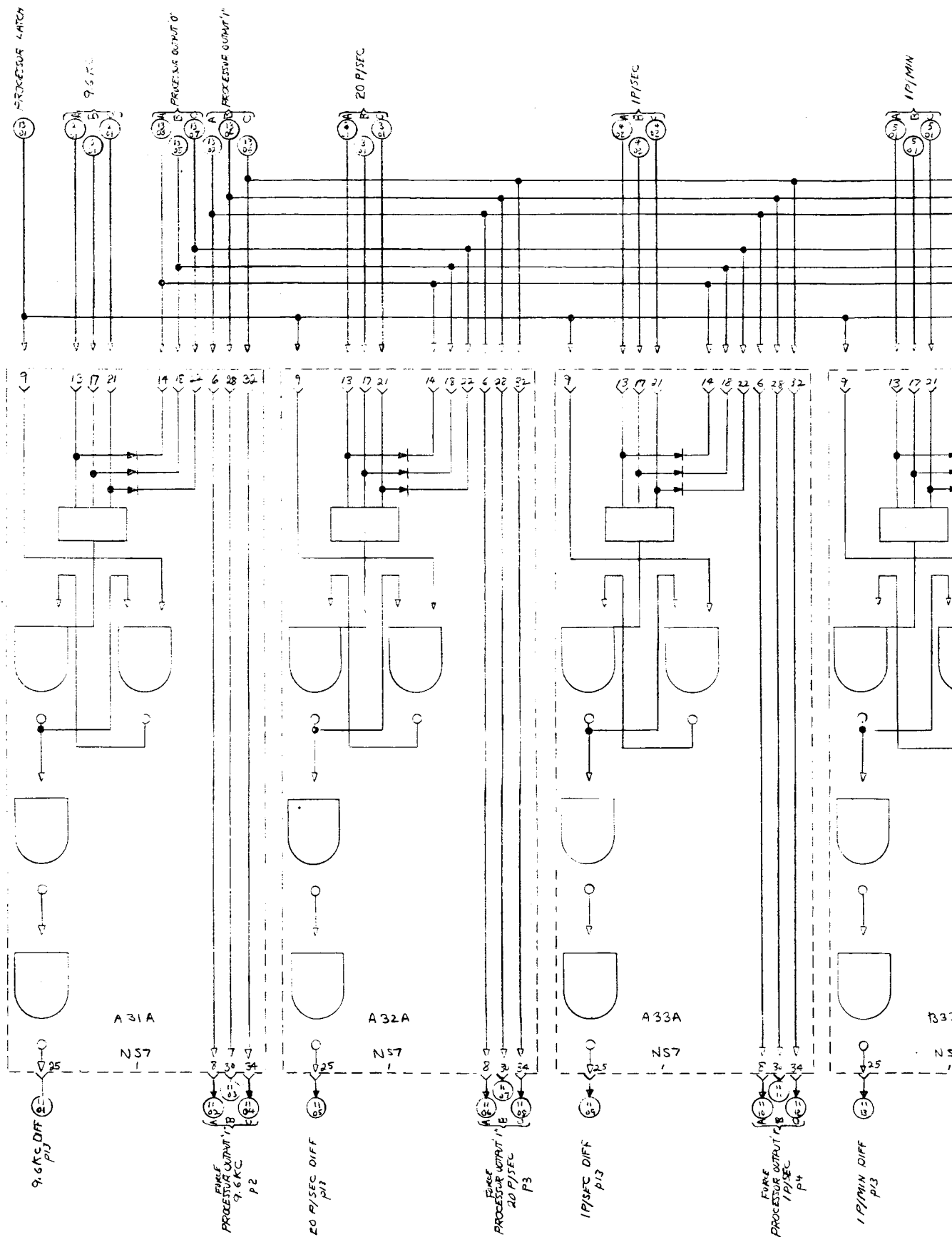
REVISIONS

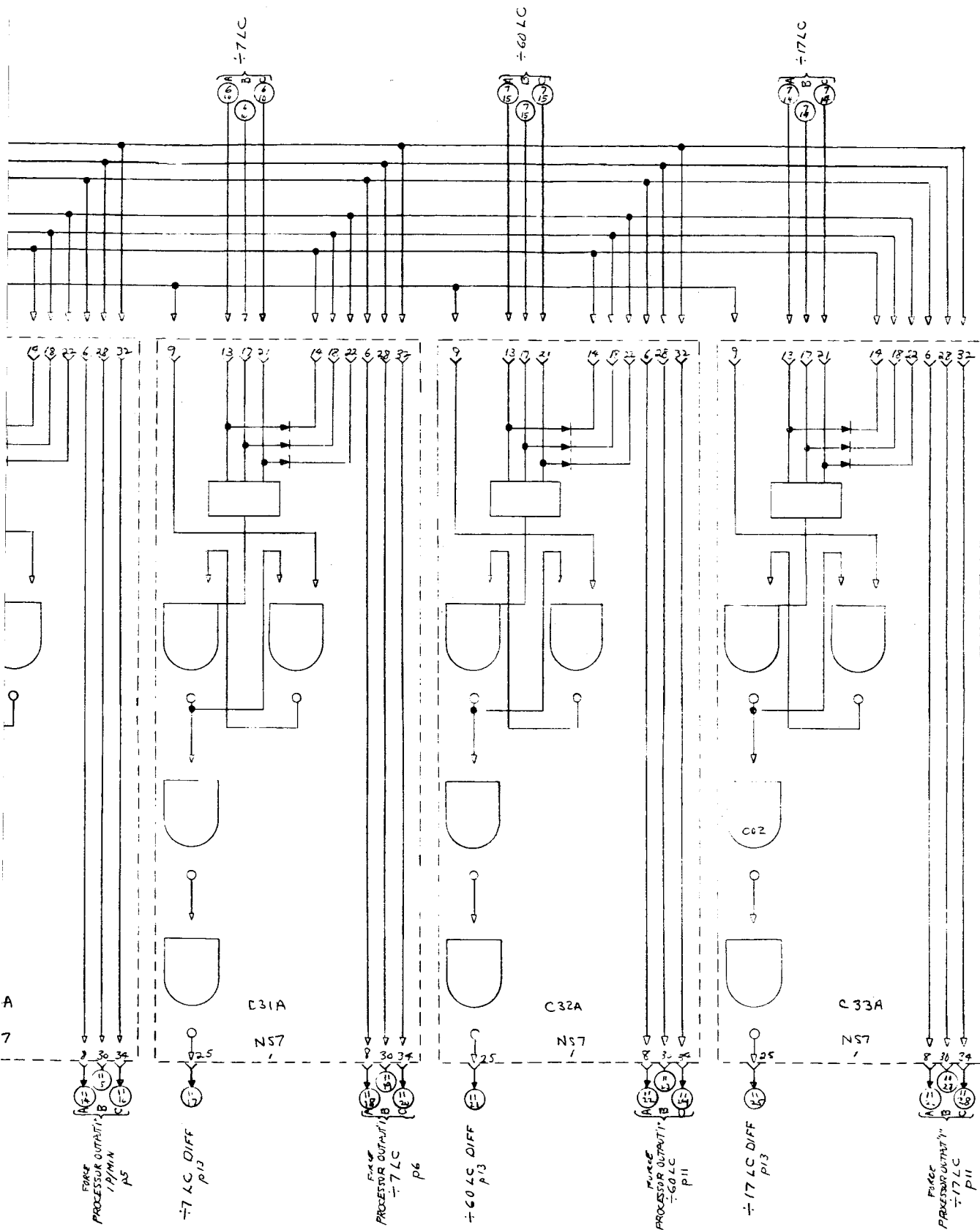




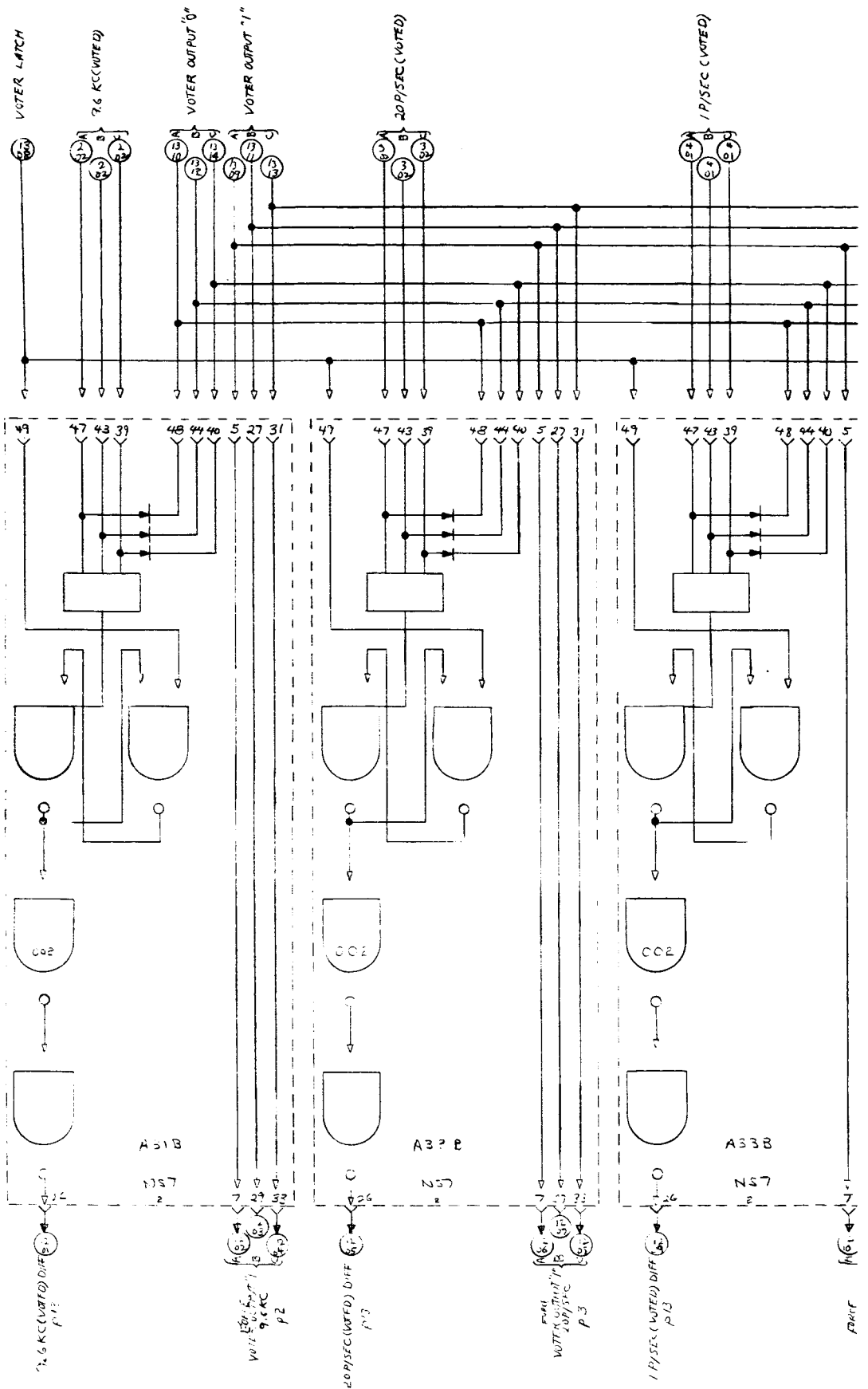
2

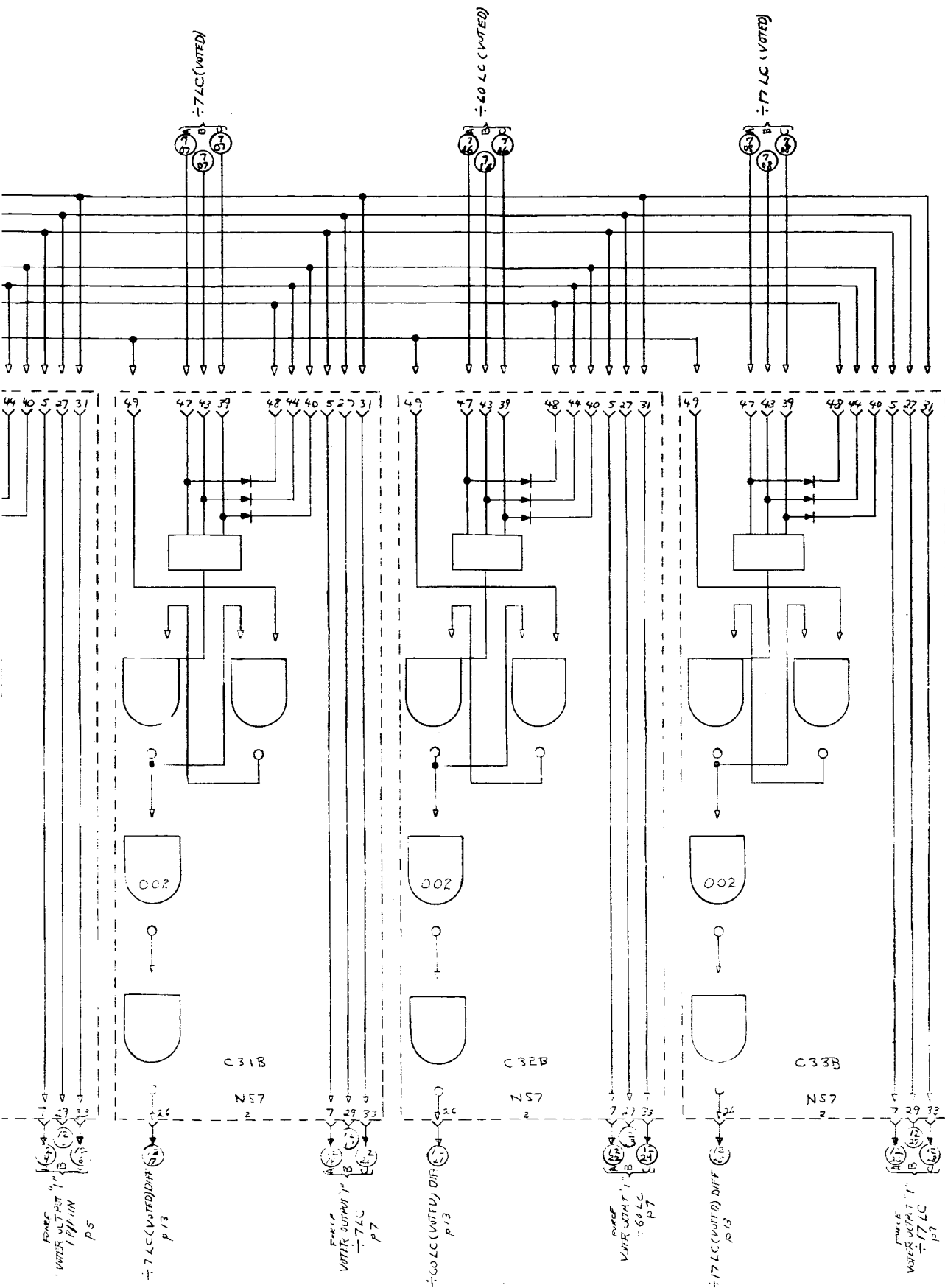
DESIGNED APPROVED CHARGE	ENGINEERING SKETCH	WESTINGHOUSE ELECTRIC CORPORATION SURFACE DIVISION BALTIMORE, MD., U. S. A. <small>DESIGNED TO BE APPROVED BY FINAL DESIGNER</small> <b>SK C</b> SHEET 10 OF 14 SHEETS
	TITLE	
	TEST LOGIC 1P/7HR LIGHTS, 11/7/58, CLEAR & COUNTING LIGHT INPUTS	
	FIG. 7-12/11	

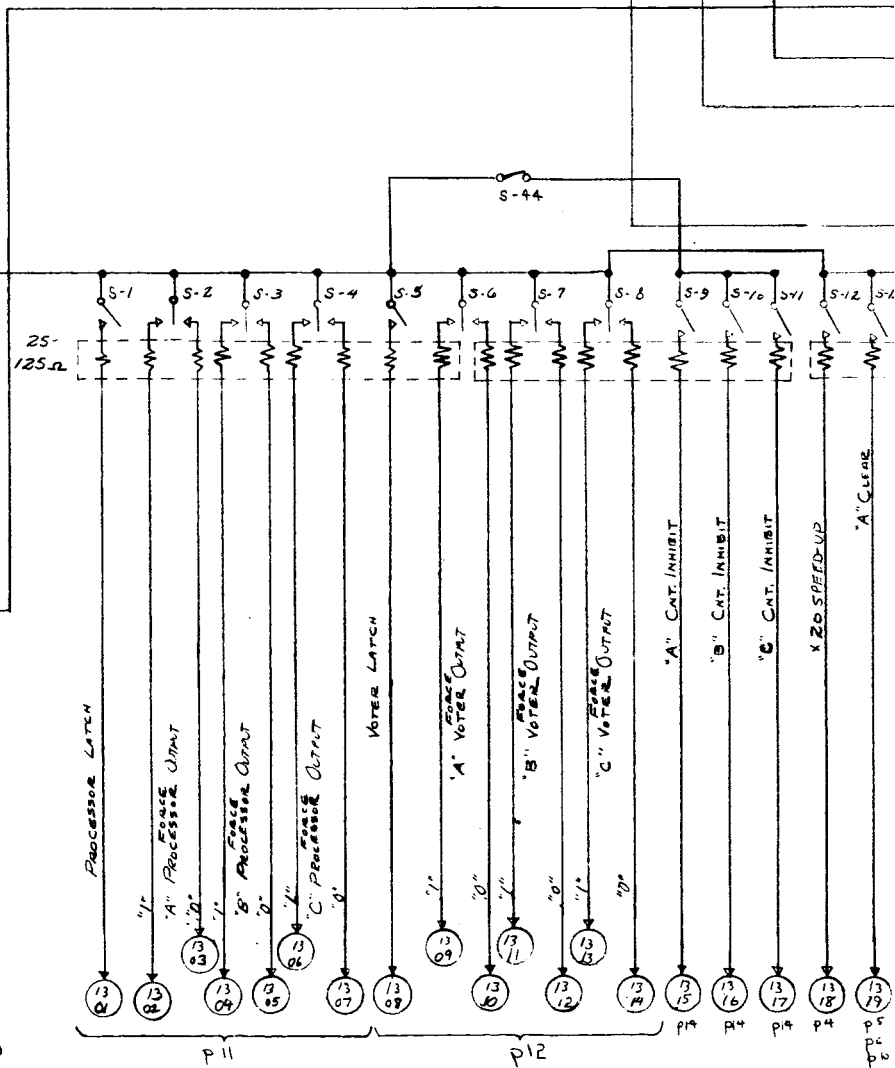
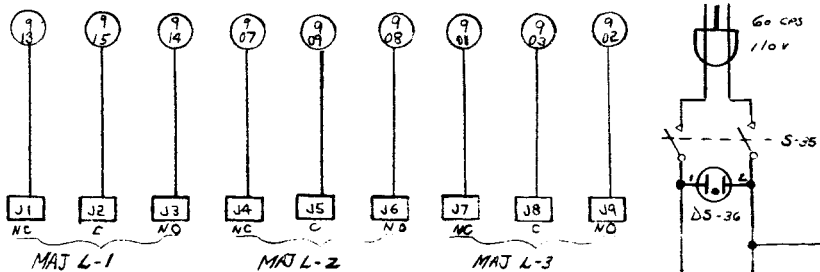
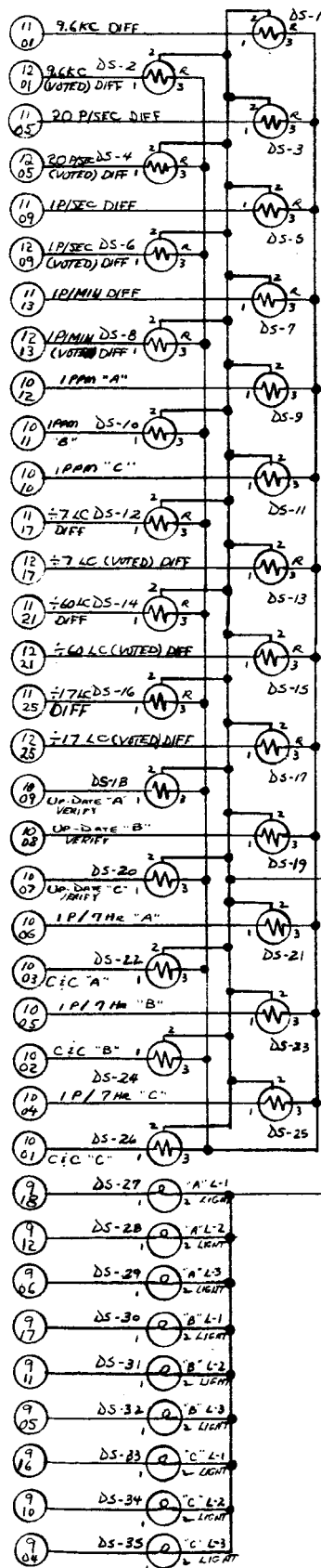




DESIGNED _____ APPROVED _____ CHECKED _____	ENGINEERING SKETCH TITLE <b>TEST LOGIC</b> <b>PROCESSOR DIFFERENCE</b> <b>DETECTORS</b> <b>FIG. 7-12/2</b>	<b>WESTINGHOUSE</b> <b>ELECTRIC</b> <b>CORPORATION</b> SURFACE DIVISION BALTIMORE, MD., U. S. A. SK <b>C</b> SHEET 11 OF 14 SHEETS
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INPUT 1 2 3 GND R(10) +12V DC TRANSISTORIZED NEON

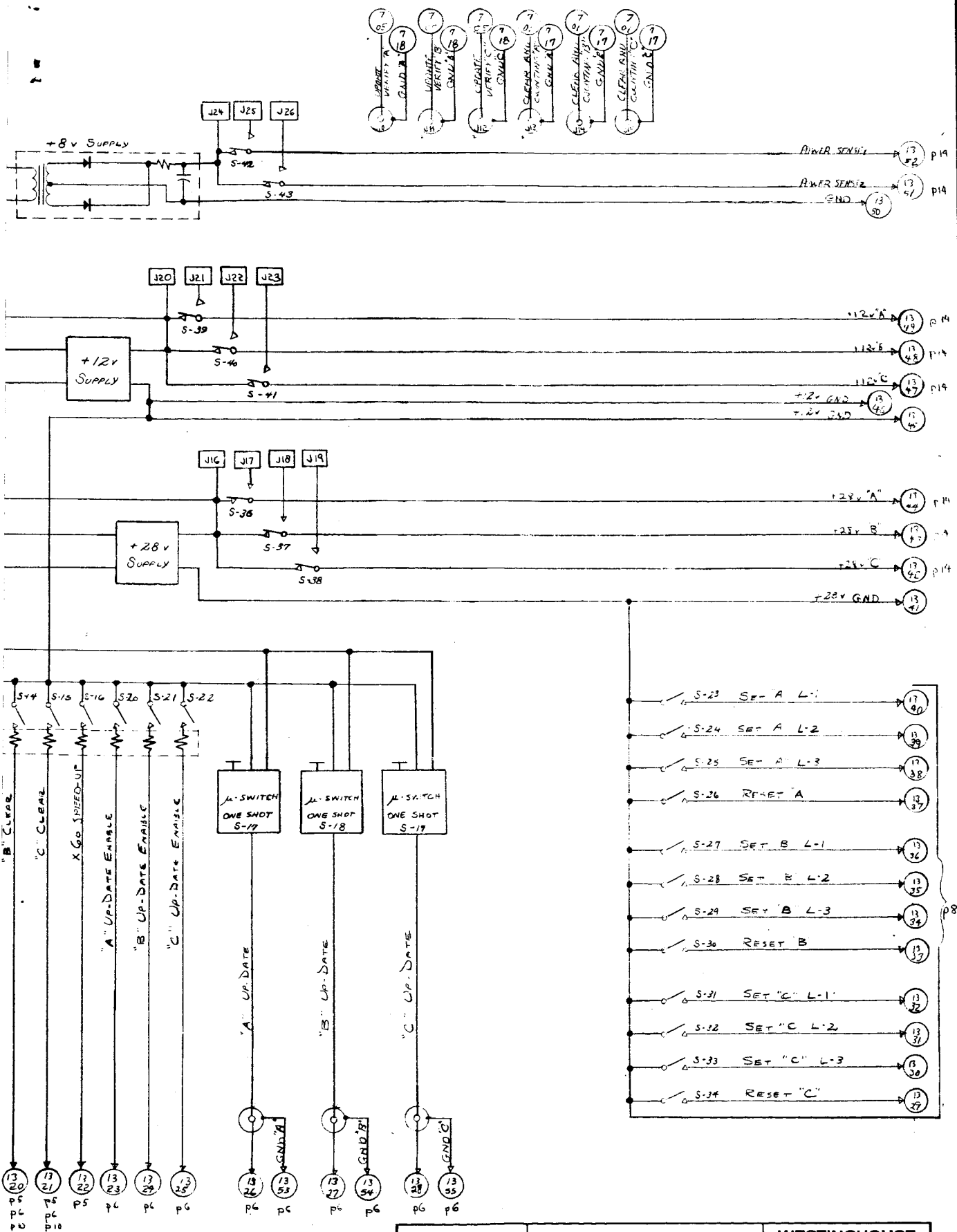
INPUT 1 2 3 +28V DC 28V INCANDESCENT

1 2 3 110V AC NEON

J3 TEST POINT

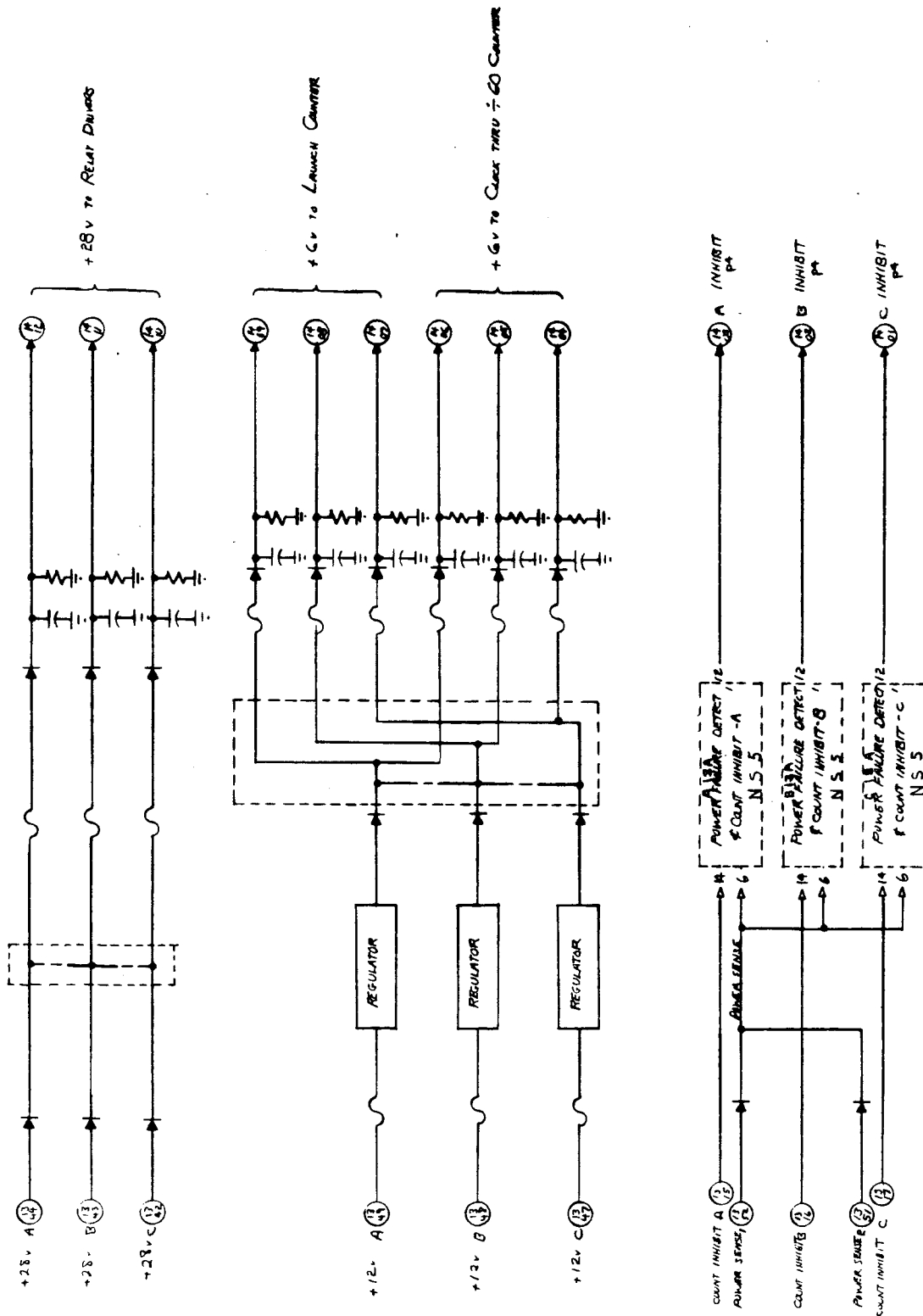
J11 COAX TEST POINT

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2

ENGINEERING SKETCH		WESTINGHOUSE ELECTRIC CORPORATION SURFACE DIVISION BALTIMORE, MD., U. S. A.
TITLE TEST CHASSIS SCHEMATIC		
DATE	APPROVED	SK C
CHARGE		FIG. 7-13
		SHEET 13 OF 14 SHEETS



ENG APPROVED CHARGE	ENGINEERING SKETCH	WESTINGHOUSE ELECTRIC CORPORATION SURFACE DIVISION BALTIMORE, MD., U. S. A. SK B SHEET 14 OF 14 SHEETS
	TITLE	
	POWER DISTRIBUTION SEQUENCER CHASSIS	
	Fig. 7-14	

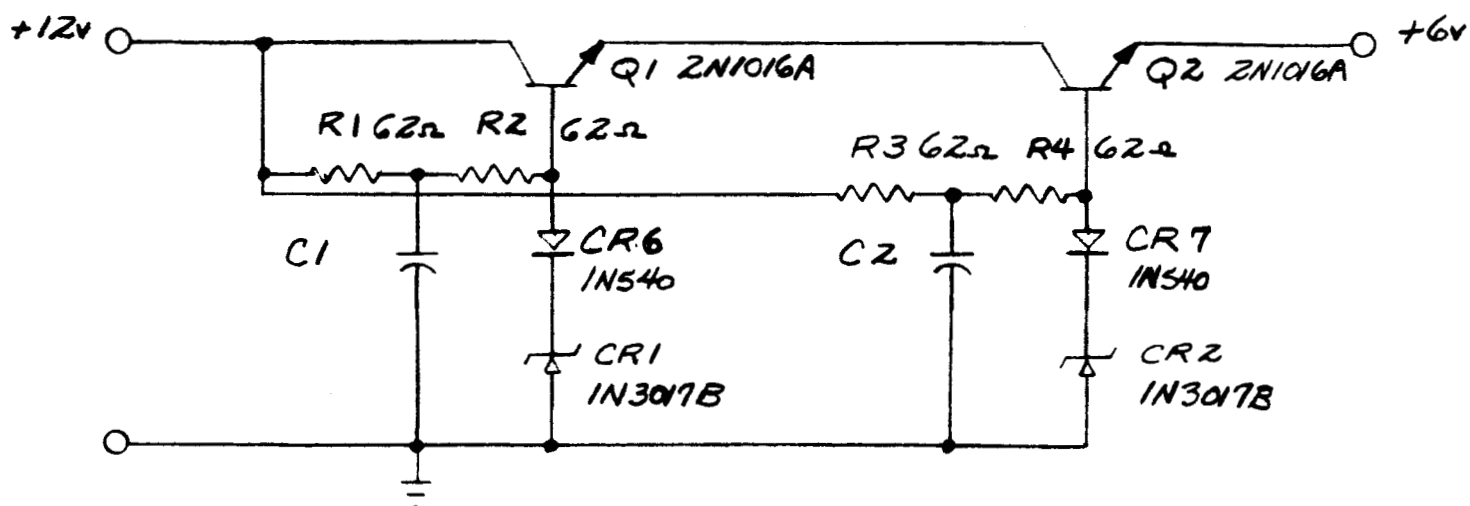


Fig. 7-14/2. Power Distribution, Regulator.

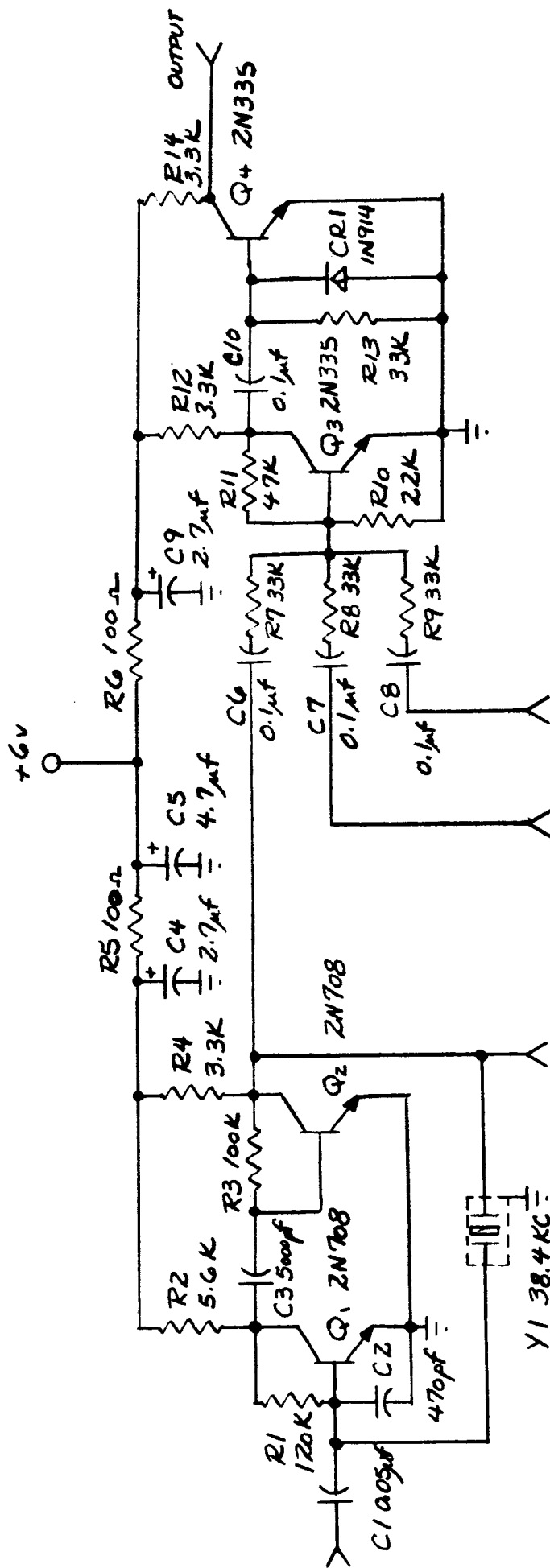
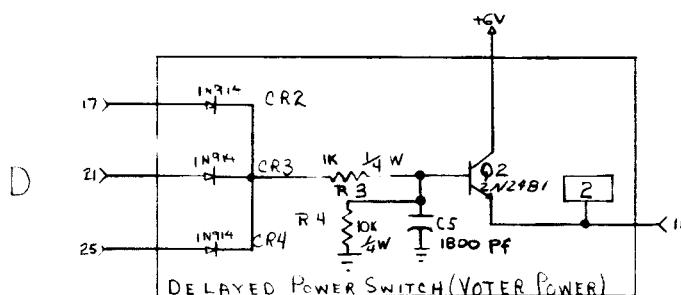
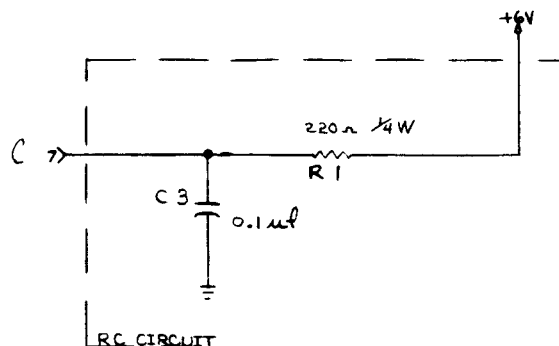
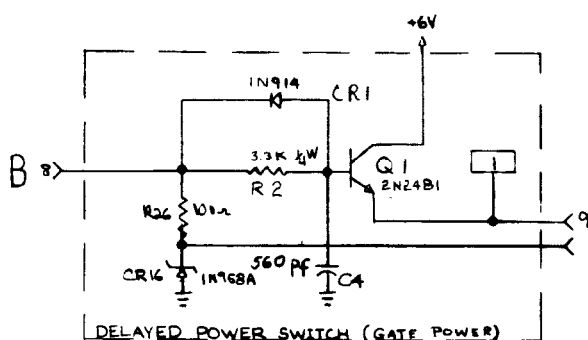
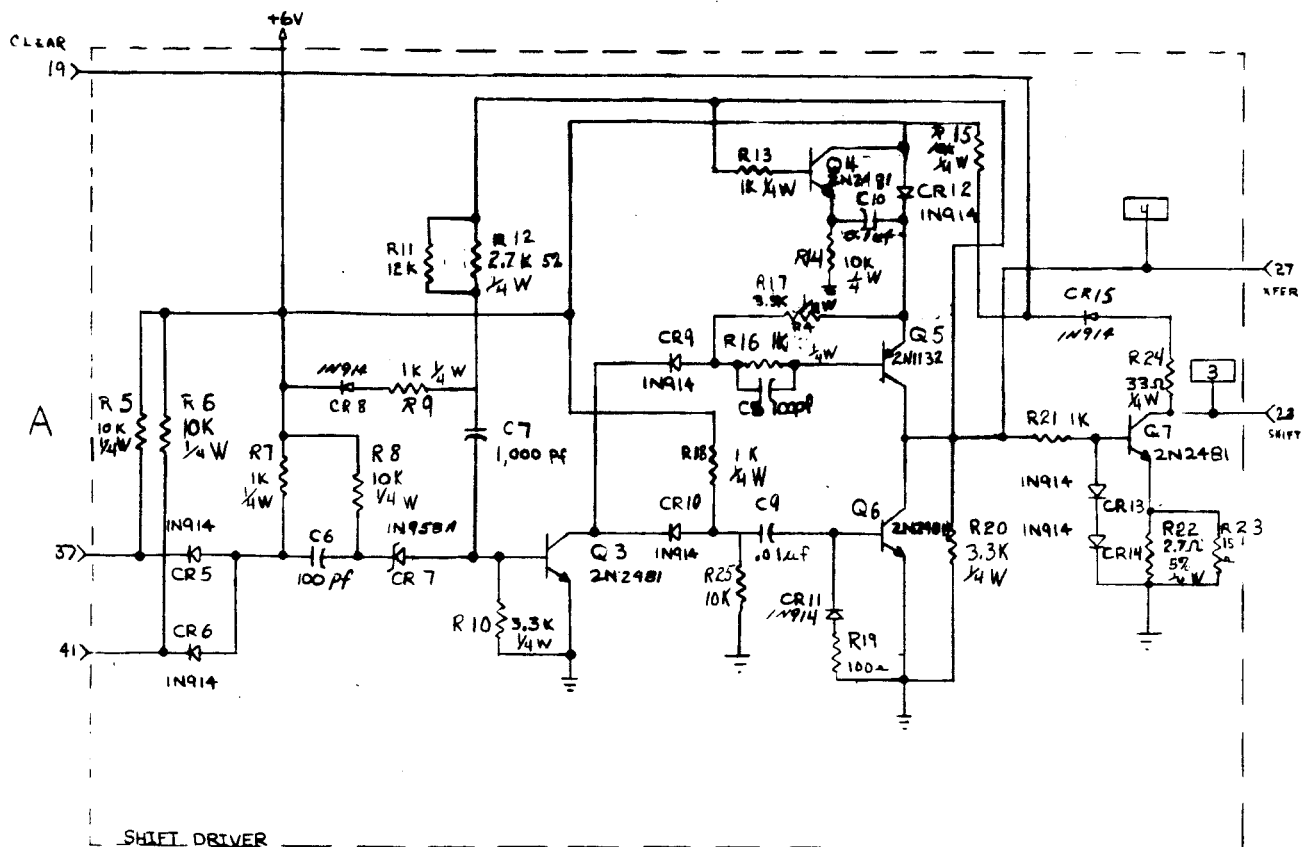
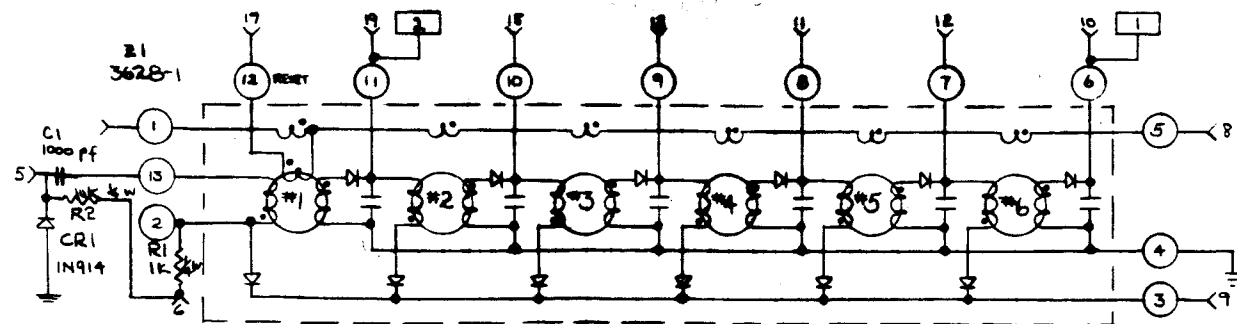


Fig. 7-15. Redundant Clock Source

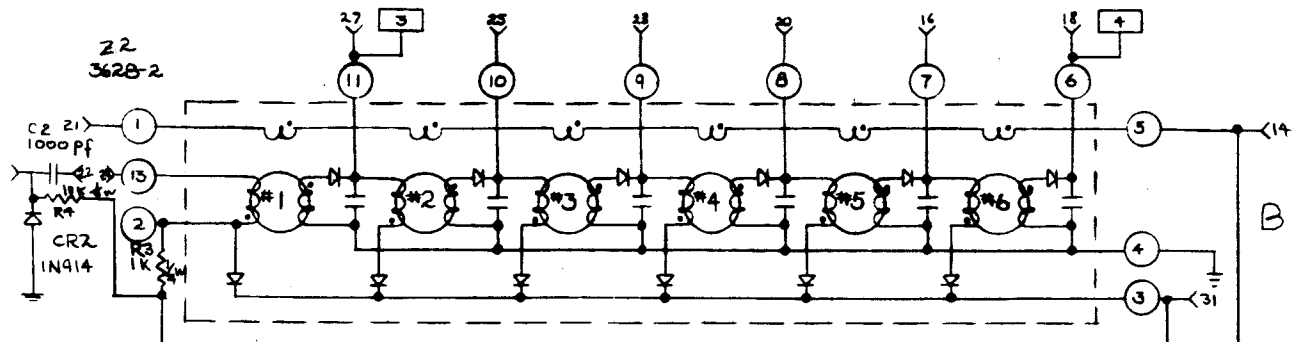


NOTE ALL RESISTORS 1/4 W UNLESS OTHERWISE SPECIFIED

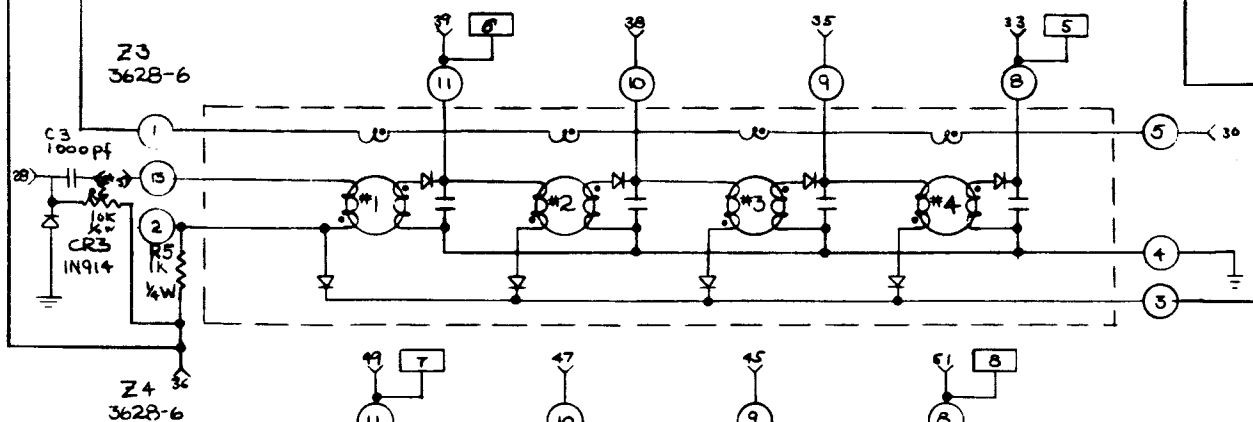
REVISIONS ENG _____ APPROVED _____ CHARGE _____	ENGINEERING SKETCH	WESTINGHOUSE ELECTRIC CORPORATION SURFACE DIVISION BALTIMORE, MD., U. S. A. NUMBER TO BE ASSIGNED TO FINAL DRAWING SK B SHEET 2 OF 11 SHEETS
	TITLE	
	NS2	
	SHIFT DRIVER	
	DELAYED POWER SWITCHES	
	RC CIRCUIT	
	FIG 7-16	



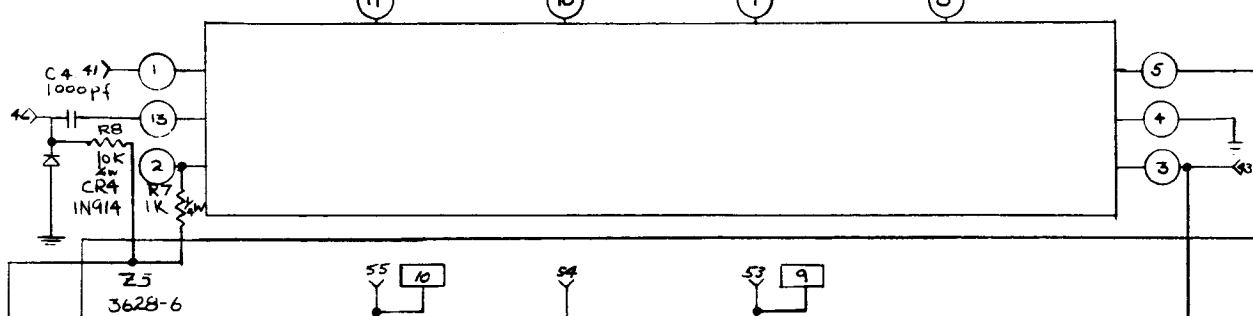
A



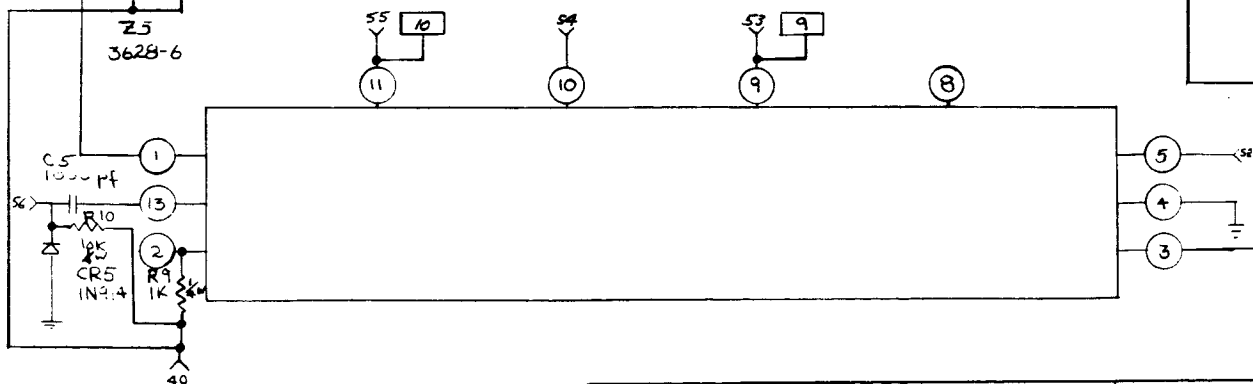
B1



B2



C1

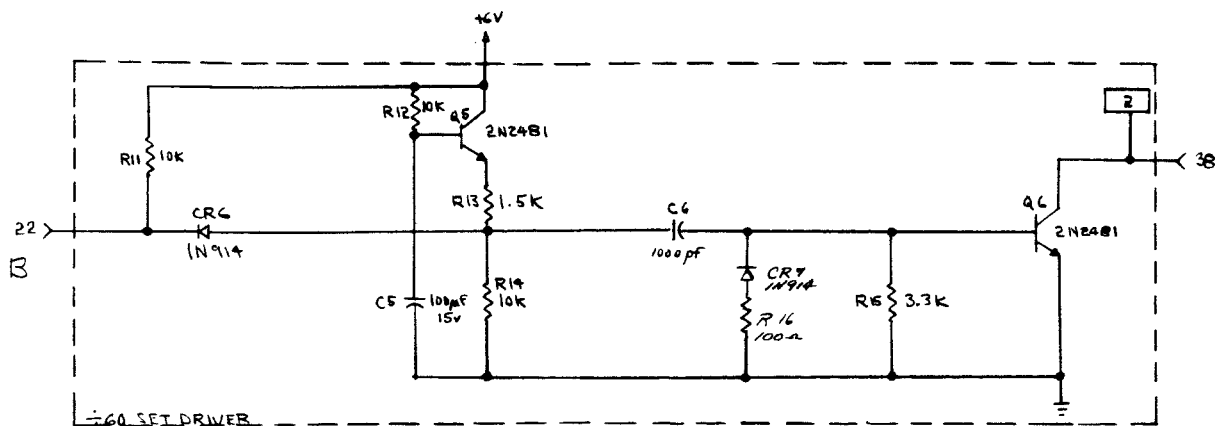
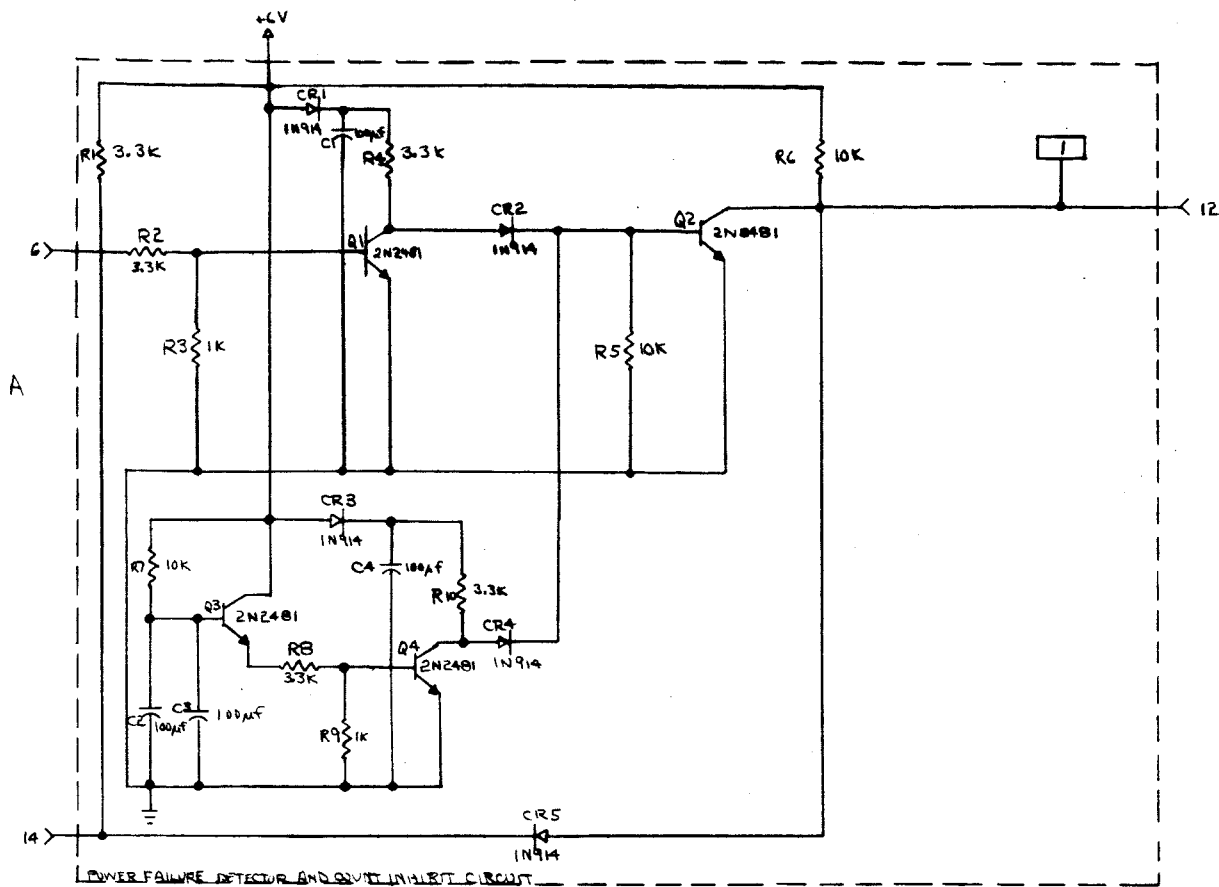


C2

REVISIONS NO. _____ APPROVED _____ CHARGE _____	ENGINEERING SKETCH	WESTINGHOUSE ELECTRIC CORPORATION SURFACE DIVISION BALTIMORE, MD., U. S. A. SK B SHEET 3 OF 11 SHEETS
	TITLE NS3	
	MAGNETIC REGISTERS	
	FIG. 7-17	

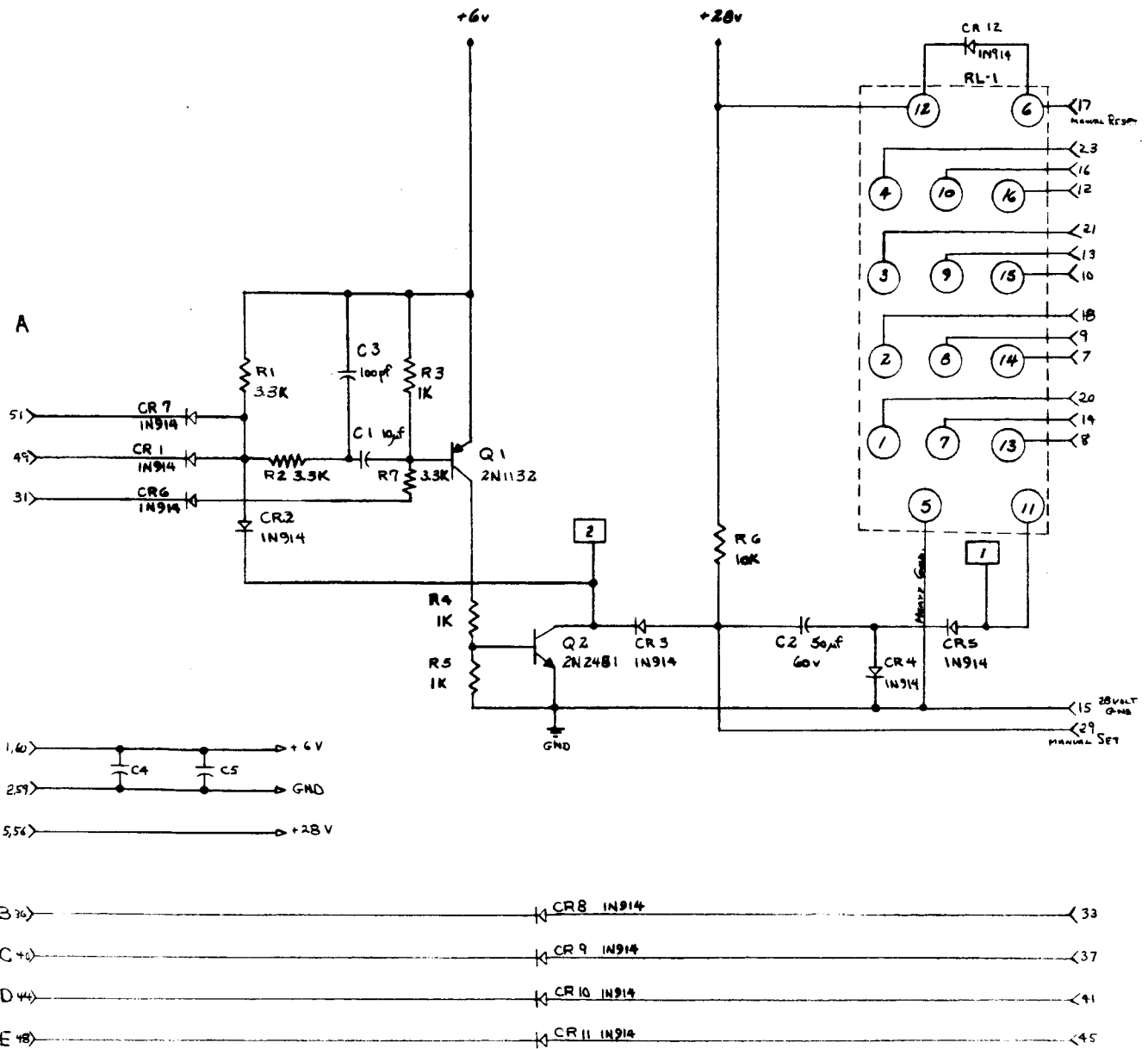


ENG _____ APPROVED _____ CHARGE _____	ENGINEERING SKETCH TITLE <b>NS4</b> <b>BUFFERS</b>	<b>WESTINGHOUSE</b> <b>ELECTRIC</b> <b>CORPORATION</b> SURFACE DIVISION BALTIMORE, MD., U. S. A.
		NUMBER TO BE APPROVED TO FINAL DRAWING <b>SK</b> <b>B</b>
	<b>FIG. 7-18</b>	SHEET <b>4</b> OF <b>11</b> SHEETS



NO. OF LOTS 1/4 INCH

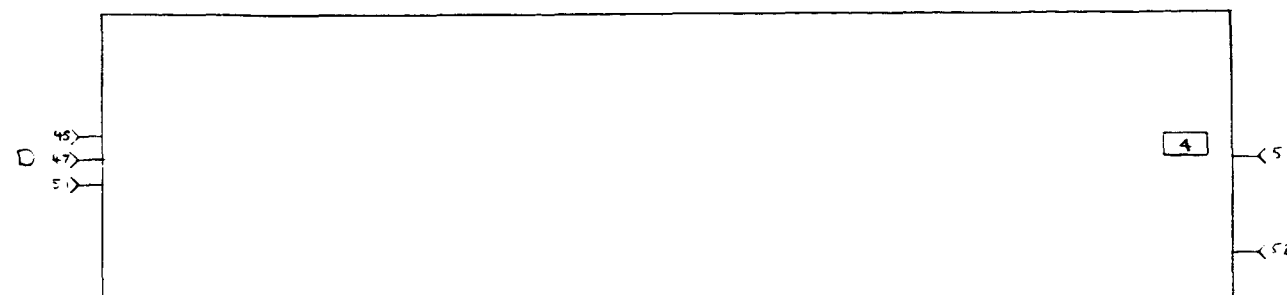
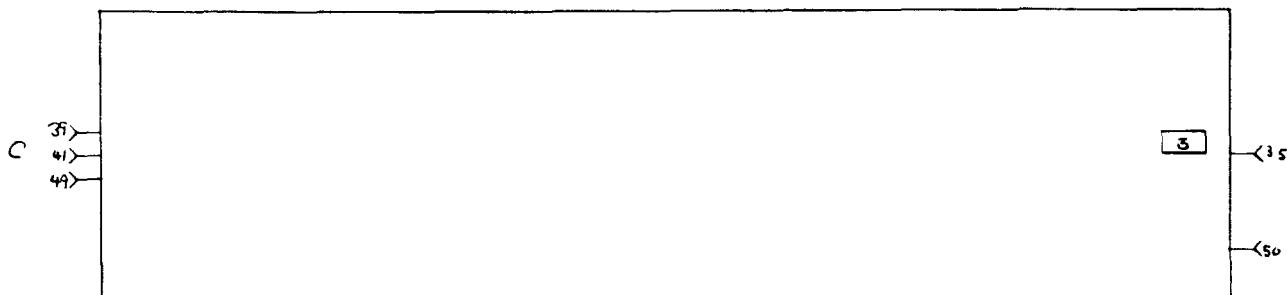
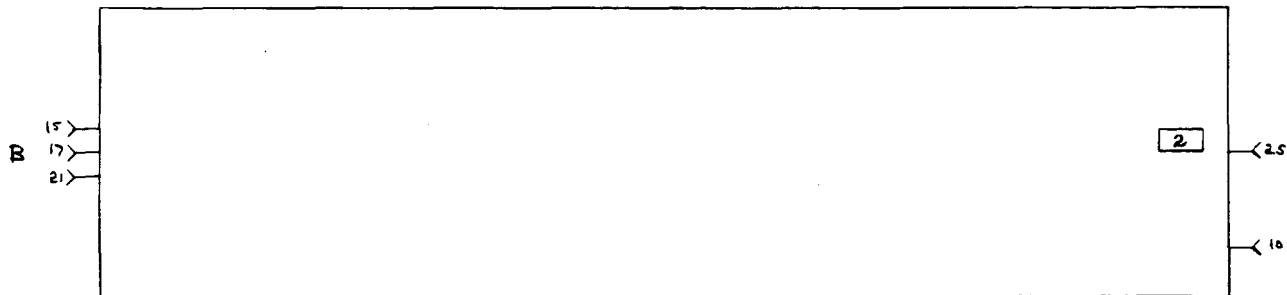
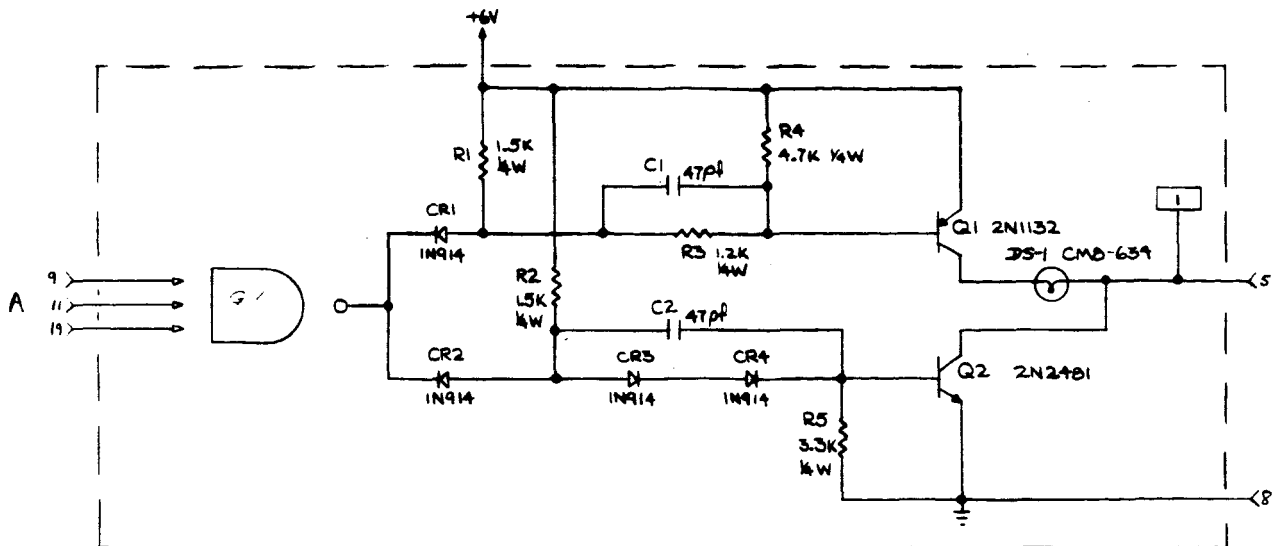
DES APPROVED CHARGE	ENGINEERING SKETCH	<b>WESTINGHOUSE ELECTRIC CORPORATION</b> SURFACE DIVISION BALTIMORE, MD., U. S. A. <small>DESIGNED TO BE ASSIGNED TO FINAL DESIGN</small> <b>SK B</b> SHEET 5 OF 11 SHEETS
	TITLE	
	N55 POWER FAILURE DETECTOR & QUINT INHIBIT CIRCUIT -60 SET DRIVER FIG. 7-19	



ALL RESISTORS 1/4W UNLESS OTHERWISE SPECIFIED

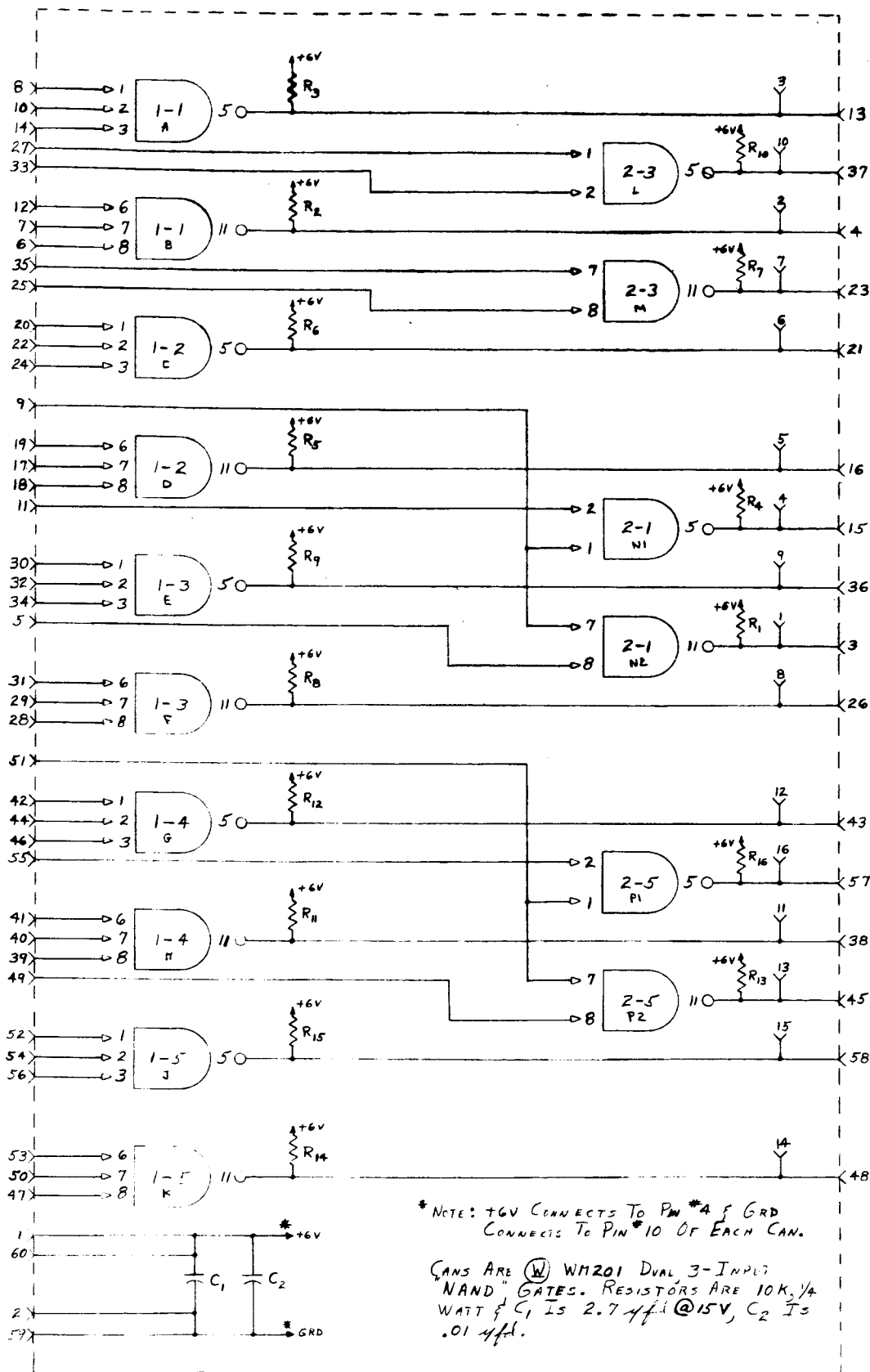
DESIGNED APPROVED CHARGE	ENGINEERING SKETCH	<b>WESTINGHOUSE ELECTRIC CORPORATION</b> SURFACE DIVISION BALTIMORE, MD., U. S. A. SK B SHEET 6 OF 11 SHEETS
	TITLE NSG	
	RELAY DRIVER AND DIODE ARRAY	
Fig. 7-20		





NEXT ASSY 330D469

ENG _____ APPROVED _____ CHARGE _____	ENGINEERING SKETCH	<b>WESTINGHOUSE ELECTRIC CORPORATION</b> SURFACE DIVISION BALTIMORE, MD., U. S. A. NUMBER TO BE ASSIGNED IN FINAL DRAWING <b>SK B</b>
	TITLE 469 LINE DRIVER	
	FIG. 7-22	
SHEET 8 OF 11 SHEETS		



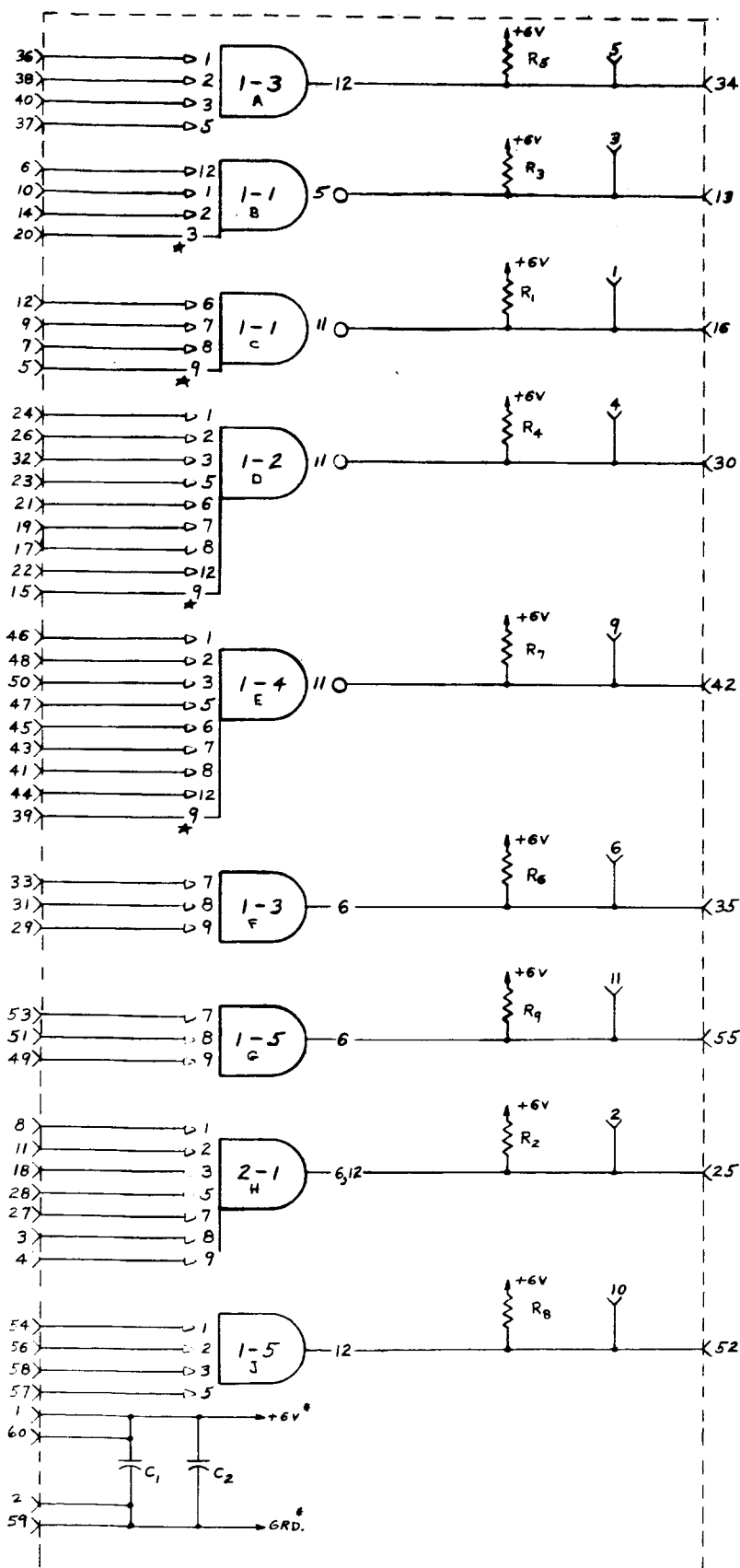
NEXT Assy 3304002

7/1/62  
DESIGNED BY F. J. [Signature]  
APPROVED \_\_\_\_\_  
CHANGE 33518

ENGINEERING SKETCH  
TITLE LOGIC DIAGRAM,  
GATE, NAND.  
FIG. 7-23

WESTINGHOUSE  
ELECTRIC  
CORPORATION  
SURFACE DIVISION  
BALTIMORE, MD., U. S. A.  
SK127.C 628  
SHEET 9 OF 11 SHEETS

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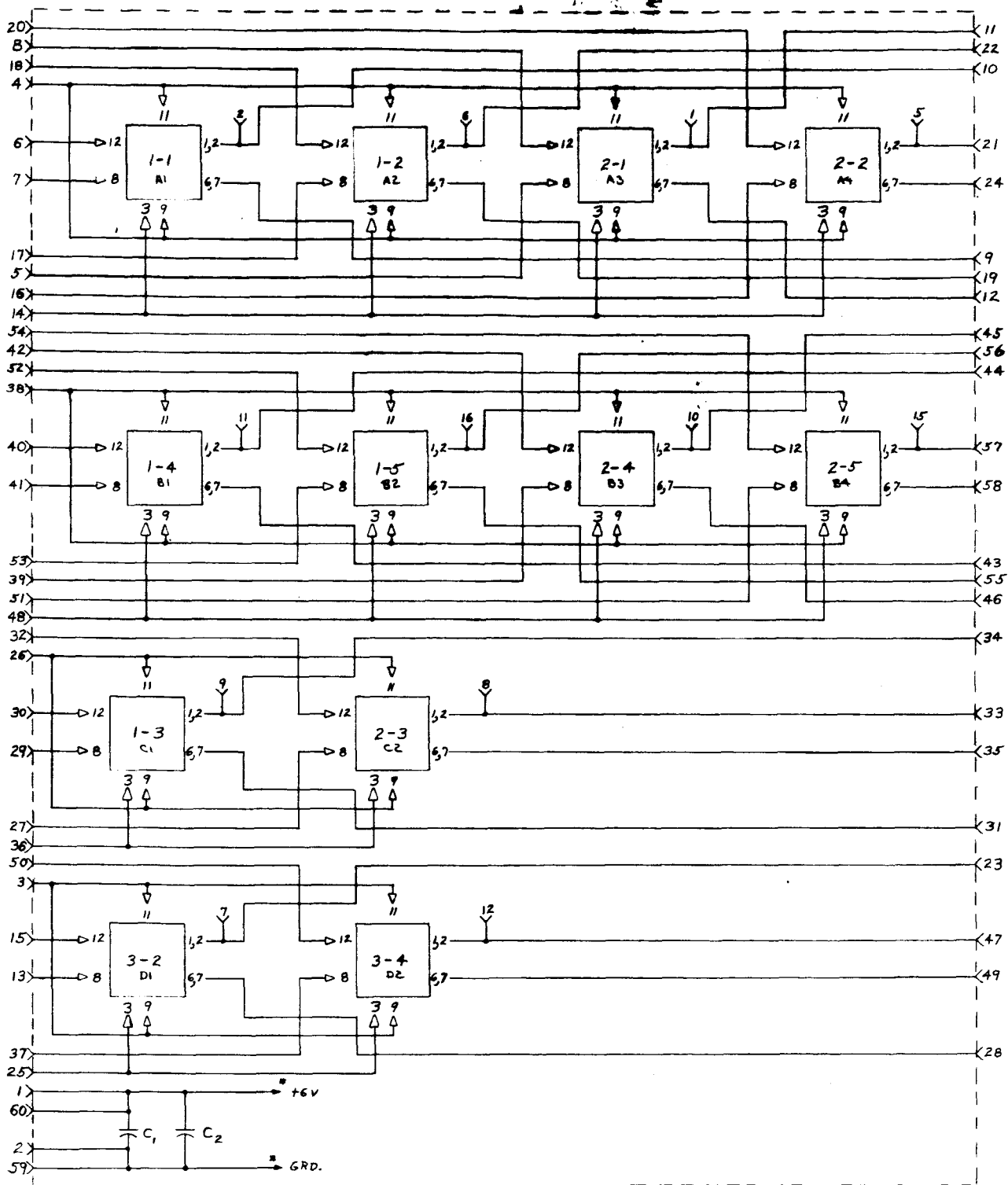
CAN POSITION 1-1 IS (W)  
 WH221T, CAN POSITIONS  
 1-2 & 1-4 ARE (W) WH224T  
 & CAN POSITIONS 1-3, 1-5 & 2-1  
 ARE (W) WH217T. RESISTORS  
 ARE 10K, 1/4 W & C<sub>1</sub> IS 2.7 μF  
 @ 15V, C<sub>2</sub> IS .01 μF.

\* NOTE: +6V CONNECTS TO PIN #4 &  
 GRD CONNECTS TO PIN #10 OF  
 EACH CAN.

\* NOTE: INPUTS TO GATES WITHOUT  
 ARROWS DENOTE NODES.

NEXT ASSY 330 D014

7/27/60 EX-100 APPROVED CHARGE 3357B	ENGINEERING SKETCH	WESTINGHOUSE ELECTRIC CORPORATION SURFACE DIVISION BALTIMORE, MD., U. S. A. SK127C 801
	TITLE	
	LOGIC DIAGRAM, GATE, FAN-IN	
	FIG. 7-24	
SHEET 10 OF 11 SHEETS		



\* NOTE: +6V CONNECTS TO PIN #4 & GRD CONNECTS TO PIN #10 OF EACH MED CAN.

CAN: ARL (W) \* WM215 J-K FLIP-FLOPS,  $C_1$  IS  $2.7\mu F @ 15V$  &  $C_2$  IS  $.01\mu F$ .

NEXT ASS'y 330DC04

7/17/63 BY <i>F. L. Smith</i> APPROVED _____ CHARGE 33518	ENGINEERING SKETCH TITLE LOGIC DIAGRAM, REGISTER, PARALLEL.	WESTINGHOUSE ELECTRIC CORPORATION SURFACE DIVISION BALTIMORE, MD., U. S. A. SK 127C 629
	FIG. 7-25	SHEET 11 OF 11 SHEETS

TABLE 7-26. CARD ASSIGNMENT

<u>SLOT NUMBER</u>			<u>CARD TYPE</u>
REPLICA A	REPLICA B	REPLICA C	
01	01	01	SPACE
02	02	02	002
03	03	03	004
04	1	1	014
05	1	1	002
06	1	1	NS2
07	1	1	SPACE
08	1	1	NS3
09	1	1	NS4
10	1	1	NS4
11	1	1	002
12	1	1	NS2
13	1	1	NS5
14	1	1	002
15	1	1	NS2
16	1	1	SPACE
17	1	1	NS3
18	1	1	NS4
19	1	1	NS4
20	1	1	002
21	1	1	002

Replica B & Replica C are same as Replica A through Slot Number 30.

TABLE 7-26. CARD ASSIGNMENT (Continued)

<u>SLOT NUMBER</u>			<u>CARD TYPE</u>
REPLICA A	REPLICA B	REPLICA C	
22			469
23			SPACE
24			NS6
25			SPACE
26			NS6
27			SPACE
28			NS6
29	29	29	D30
30	30	30	SPACE
31			NS7
32			NS7
33			NS7
	31		SPACE
	32		004
	33		NS7
		31	NS7
		32	NS7
		33	NS7

TABLE 7-27. PARTS LIST, SEQUENCER CHASSIS

<u>Part</u>	<u>Quantity</u>
Card-Rack Assembly, Trio Metal Products	1
Dust Cover	1
Base	1
Card Connector, Hughes #EMS030DJ000	80
P.C. Card NS2	9
NS3	6
NS4	12
NS5	3
NS6	9
NS7	7
NS8	3
002	18
004	4
014	3
030	3
469	3
Redundant +6V Regulator	3
Crystal Oscillator	3
Chassis Connector, Amphenol #26-4401-16P	1
Amphenol #57-40500	2
Amphenol #57-40240	1

TABLE 7-27. PARTS LIST, SEQUENCER CHASSIS (Continued)

<u>Part</u>	<u>Quantity</u>
Fuse, 1/4 amp, SLO-BLO	12
Diode, IN547	9
IN1200	6
IN3997A 5.6v	1
Resistor, RC20GF751J	9
15 OHM, 10 watt, wire wound	1
Capacitor	9

TABLE 7-28. PARTS LIST, TEST CHASSIS

<u>Part</u>	<u>Quantity</u>
Turret Chassis, Bud Type 60-2366	1
Chassis Panel, Bud Type PA-1106	1
Chassis Panel, Bud Type PA-1112	1
Chassis Panel, Bud Type PS-1259	1
+28V, Unregulated Power Supply, Acopian Model US-28	1
+12V. Regulated Power Supply, Lambda Model IMC12	1
+6V. Unregulated Power Supply	1
Transformer	1
Diode	2
Resistor	1
Capacitor	1
Fuse	1
Transistorized Indicator Light and Socket, TEC #LVN-D12-AL-F3	7
TEC #LVN-D12-AL-F3	7
TEC #LVN-D12-AL-F8	12
Incandescent Indicator Light and Socket, Dailco 101-3830-931	9
Neon Indicator Light and Socket, Dailco 133-8836-931	1
Micro Switch Push Button "One-Shot", Honeywell #1PB625	3
Push Button, Grayhill #4001	15
Toggle Switch, SPST Arror, Hart & Hegeman #6200	11
SPDT Arror, Hart & Hegeman #6202	8
SPDT-Center Off, Kulka #ST42E	6
DPDT Arror, Hart & Hegeman #6206	1

TABLE 7-28. PARTS LIST, TEST CHASSIS (Continued)

<u>Part</u>	<u>Quantity</u>
Test Point, Per Westinghouse Drawing 328C182-H0	20
Miniature Coax per Westinghouse Drawing 54B7128-H02	6
Chassis Connector, Amphenol #26-4401-16P	1
Amphenol #57-40500	2
Amphenol #57-40240	1
Cable Connector, Amphenol#26-4301-16S	2
Amphenol#57-30500	2
Amphenol#57-30240	2

NOTE: Sequencer and Test Chassis interconnected by one 16 wire (#18 gauge) power cable, one 24 wire (#24 gauge) signal cable, two 50 wire (#24 gauge) signal cables.

TABLE 7-29. PARTS LIST, REDUNDANT CLOCK SOURCE

<u>Part</u>	<u>Quantity</u> *
Capacitor, CS13AD475K	1
CS13AD275K	2
005 uf Ceramic Disc	1
0.1 uf Ceramic Disc	4
470 pf Dura Mica	1
5000 pf Dura Mica	1
Diode, 1N914	1
Transistor, 2N335	2
2N2481	2
Resistor, RCO7GF123K	1
RCO7GF562K	1
RCO7GF104K	1
RCO7GF332K	3
RCO7GF101K	2
RCO7GF333K	4
RCO7GF223K	1

\* For one of the three interconnected circuits used.

TABLE 7-30. PARTS LIST, CARD TYPE NS2

<u>Part</u>	<u>Quantity</u>
Capacitor, CS13ED273K	1
C-23 3C3	2
CK05CW101K	2
EPC06X104-M	2
EPC04X182-M	2
CK05CW102K	1
Diode, 1N914	13
1N9S8A	2
Transistor, 2N2481	6
2N1132	1
Resistor, RCO7GF102K	6
RCO7GF332K	3
RCO7GF103K	8
RCO7GF220K	2
RCO7GF221K	1
RC20GF2R7J	1
RCO7GF272J	1
RCO7GF101K	2
RCO7GF152K	1

TABLE 7-31. PARTS LIST, CARD TYPE NS3

<u>Part</u>	<u>Quantity</u>
Capacitor, CK05CW102K	5
Diode, 1N914	5
Resistor, RC07GF102K	5
RC07GF103K	5
Magnetic Device, 6 Bit Register with Reset, C&K #3628-1	1
6 Bit Register without Reset, C&K #3628-2	1
4 Bit Register without Reset, C&K #3628-6	3

TABLE 7-32. PARTS LIST, CARD TYPE NS4

<u>Part</u>	<u>Quantity</u>
Capacitor, CS13BD275K	1
C-233C3	1
CK05CW101K	4
Diode, 1N914	28
Transistor, 2N2481	8
Resistor, RCO7GF472K	4
RCO7GF103K	13

TABLE 7-33. PARTS LIST, CARD TYPE NS5

<u>Part</u>	<u>Quantity</u>
Capacitor, CS13BD107K	5
C-233C3	2
CS13BD275K	1
Diode, 1N914	6
Transistor, 2N2481	6
2N1132	1
Resistor, RCO7GF332K	5
RCO7GF102K	3
RCO7GF103K	7
RCO7GF101K	1

TABLE 7-34. PARTS LIST, CARD TYPE NS6

<u>Part</u>	<u>Quantity</u>
Capacitor, CS13BE106K	1
CS13BD275K	1
CL65BK500MP3	1
CKOSCWL01K	1
C-233C3	1
Diode, 1N914	11
Transistor, 2N2481	1
2N1132	1
Resistor, RCO7GF332K	3
RCO7GF1C2K	3
RCO7GF103K	1
Relay, Potter and Brumfield Type TL17D	1

TABLE 7-35. PARTS LIST, CARD TYPE NS7

<u>Part</u>	<u>Quantity</u>
Capacitor, EPC044182-M	2
Diode, 1N914	18
Transistor, 2N2481	2
Resistor, RCO7GF332K	6
RCO7GF103K	8
Microelectronic Device, WS296	4

TABLE 7-36. PARTS LIST, CARD TYPE NS8

<u>Part</u>	<u>Quantity</u>
Card Connector, Hughes # EMS03ODJ000	1
Connector Mounting Block	2
Patchboard, Vector No. PB1010-1	1
Vector No. PB210-1	1
Patchboard Jumper Plug, Vector No. K2.02-1	75
Patchboard Jumper Cord, Vector No. K2.06	25

TABLE 7-37. PARTS LIST, CARD TYPE SSP469

<u>Part</u>	<u>Quantity</u>
Capacitor, CK05CW470K	8
Diode, 1N914	16
Transistor, 2N2481	4
2N1132	4
Resistor, RCO7GF152K	8
RCO7GF122K	4
RCO7GF472K	4
RCO7GF332K	4
Microelectronic Device, WM201T	2
Ballast Lamp, Chicago Miniature CM8-634	4

TABLE 7-38. PARTS LIST, NAND GATE

<u>Part</u>	<u>Quantity</u>
Capacitor, C-233C3	1
CS13BD275K	1
Resistor, RCO7GF103K	16
Microelectronic Device, WM201T	8

TABLE 7-39. PARTS LIST, FAN-IN GATE

<u>Part</u>	<u>Quantity</u>
Capacitor, C-233C3	1
CS13BD275K	1
Resistor, RC07GF103K	9
Microelectronic Device, WM217T	3
WM221T	1
WM224T	2

TABLE 7-40. PARTS LIST, PARALLEL REGISTER

<u>Part</u>	<u>Quantity</u>
Capacitor, C-233C3	1
CS13BD275K	1
Microelectronic Device, WM215T	12

TABLE 7-41. PARTS LIST, REDUNDANT POWER REGULATOR

<u>Part</u>	<u>Quantity</u>	*
Diode, 1N3017B	2	
1N540	2	
Transistor, 2N1016A	2	
Resistor, RC42GF620J	4	
Capacitor	2	

\* For one of the three Regulator circuits used.